Statistical Power Estimation on FPGAs

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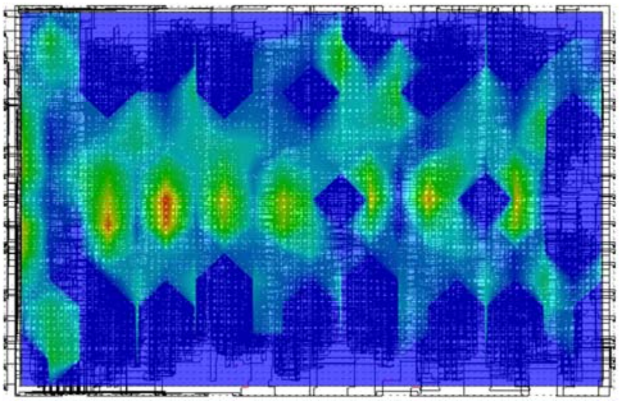
- Introduction
- The statistical approach for power estimation
- Power estimation for FPGAs
  - Activity Estimation
  - Capacitance and Power Computation
- Experiments
- Conclusions

Introduction

- Power Consumption in CMOS Circuits
  - Static Power: 5-20% (and growing fast…)
  - Dynamic Power
    - Is the most significant component and estimating it is the goal of this work.
    - Short-Circuit Power: 10% aprox. As it depends on the activity, it can be considered together with the capacitive power.
    - Capacitive Power: is the result of charging and discharging parasitic capacitances in the circuit.

Introduction

- Dynamic Power Consumption in CMOS circuits:



$$P_i = 0.5 \times V_{dd}^2 C_i A_i f_{clk}$$

$$P = 0.5 \times V_{dd}^2 f_{clk} \sum_i C_i A_i$$

Introduction

- Switching **Activity** in CMOS circuits
  - Logic Function
  - Switching Activity at Primary Inputs
  - Spatial and Temporal Dependencies among Primary Inputs
  - Circuit Structure
  - Technology-dependant factors
  - Delay Model

pattern-dependence problem

Introduction

- Classification of power estimation techniques by its target function:
  - Average Consumption
  - Maximum Consumption
    - instantaneous
    - per clock cycle
    - in n-clock cycles
    - sustainable

Introduction

- Estimation detail level:
  - Total Power Consumption
  - Individual Nodes Consumption
- Circuit Architecture:
  - Combinational
  - Sequential
- Level of Definition:
  - From algorithmic to circuit
  - Research efforts were mostly oriented to the gate level

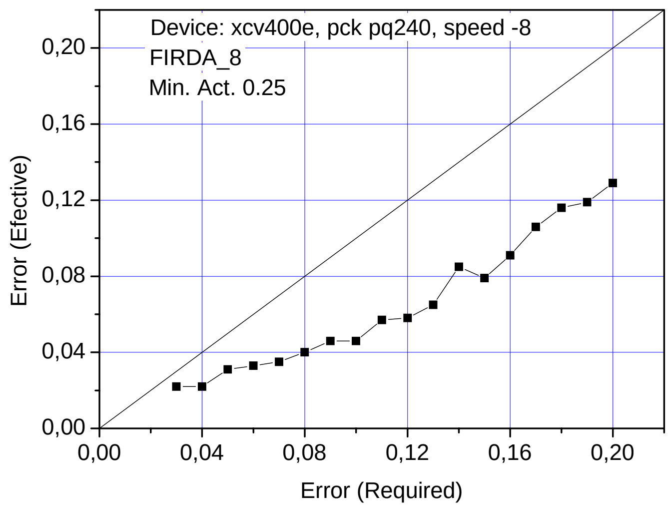
Synthesizable RTL

Introduction

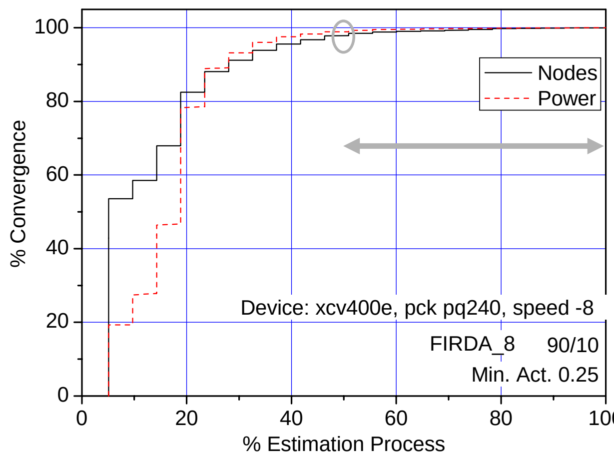
- Statistics-based Activity Estimation Techniques
- Total Power [Burch, 1993]: $N \geq \left(\frac{t_{\alpha/2} s}{p \varepsilon} \right)^2$
- Individual Nodes [Najm, 1998]:

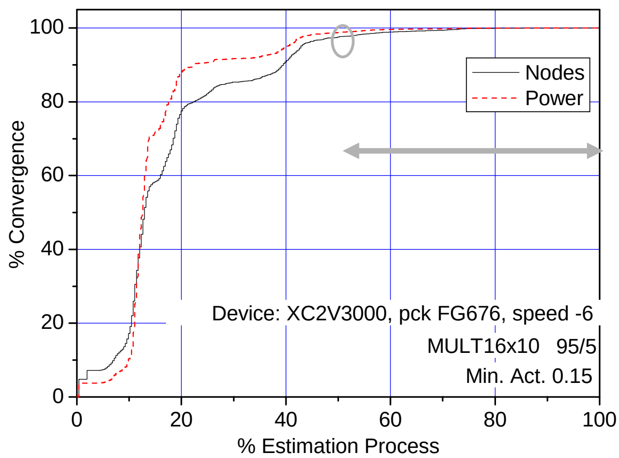
$$N \geq \left(\frac{z_{\alpha/2} s}{n_{\min} \varepsilon} \right)^2 \qquad N \geq \left(\frac{z_{\alpha/2} s}{\bar{n} \varepsilon_1} \right)^2$$

A-B Statistical Power Estimation



A-B Statistical Power Estimation





A-B Statistical Power Estimation

- The additional condition (besides the stopping criteria at the node level previously defined) to finish the estimation is:

$$\frac{N_{no}}{N_{reg}} \leq e \cdot St,$$

- Example: 10% error, 90% of confidence, 1000 normal nodes
  - If the optimization strength is 1.0, then the estimation is considered complete when more than 900 nodes have met the stopping criterion defined above.
  - If the parameter is set to 0.5, then the estimation is considered finished when more than 950 nodes have converged.

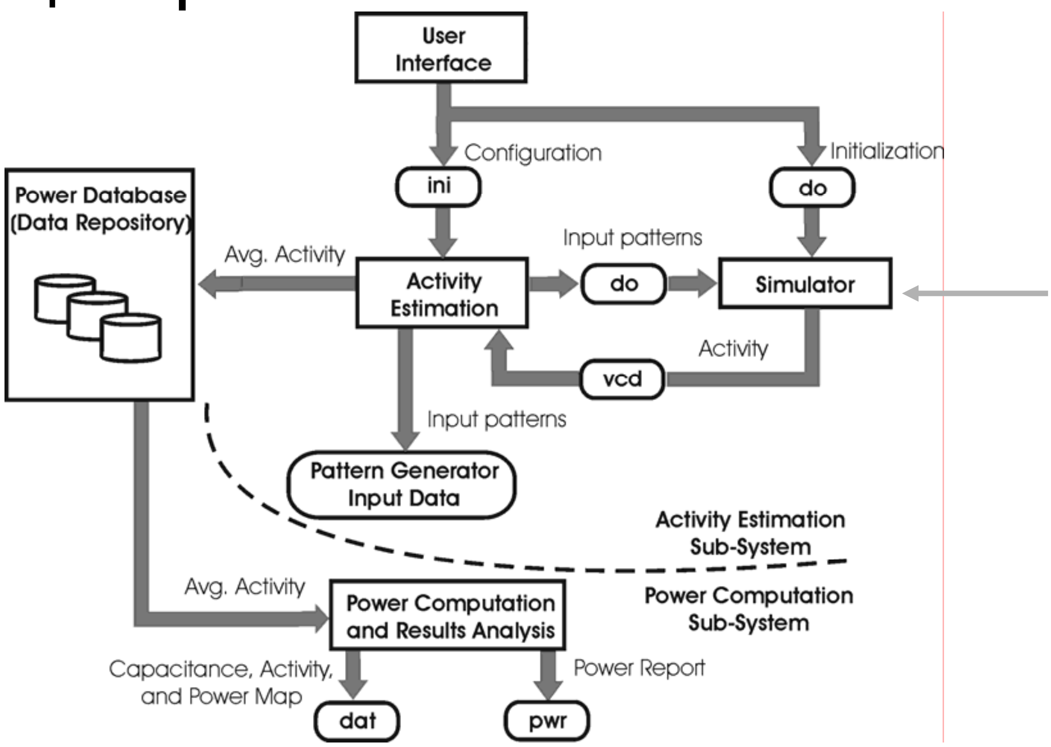
Benefits of the Statistical Approach

- Applicable to **any synthesizable level** in the design process.
- **Big circuits** can be its inputs.
- Gives a solution for the **pattern-dependence problem**.
- Any **standard simulator** can be used in the inner loop of the estimation program making the technique relatively easy to implement.

Benefits of the Statistical Approach (cont.)

- If the tolerated error is not selected too small, the **execution time** is such that the technique can be used in practice.
- A **simple input** specification can be defined.
- **Temporal and spatial correlations** are considered by the simulator for the internal nodes and temporal correlations can be specified by the user at primary inputs.
- **Glitches** are considered, if an accurate delay model is provided to the simulator.
  - Post Map, Place or Place&Route HDL model

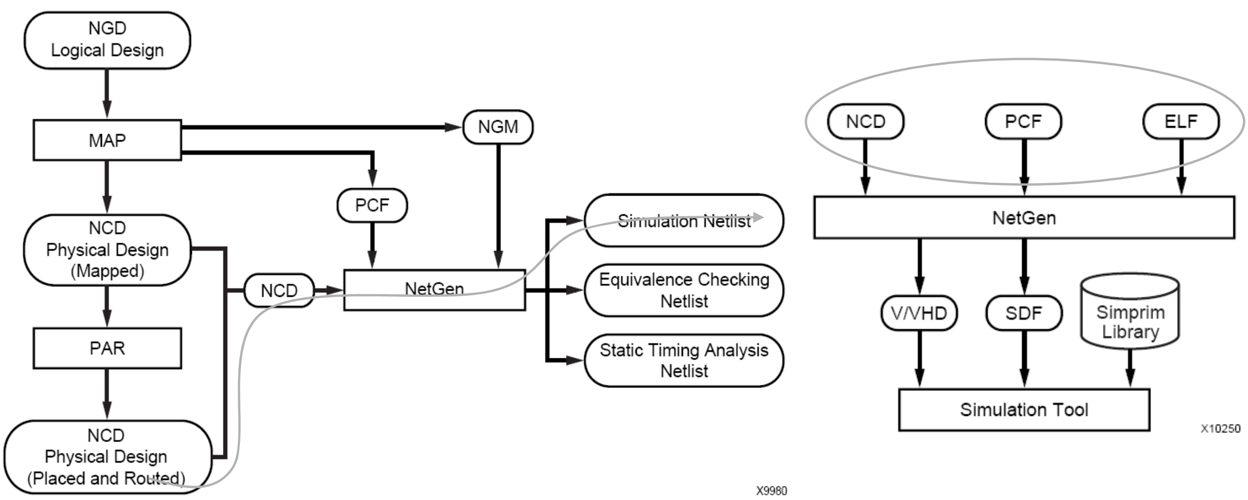
Implementation



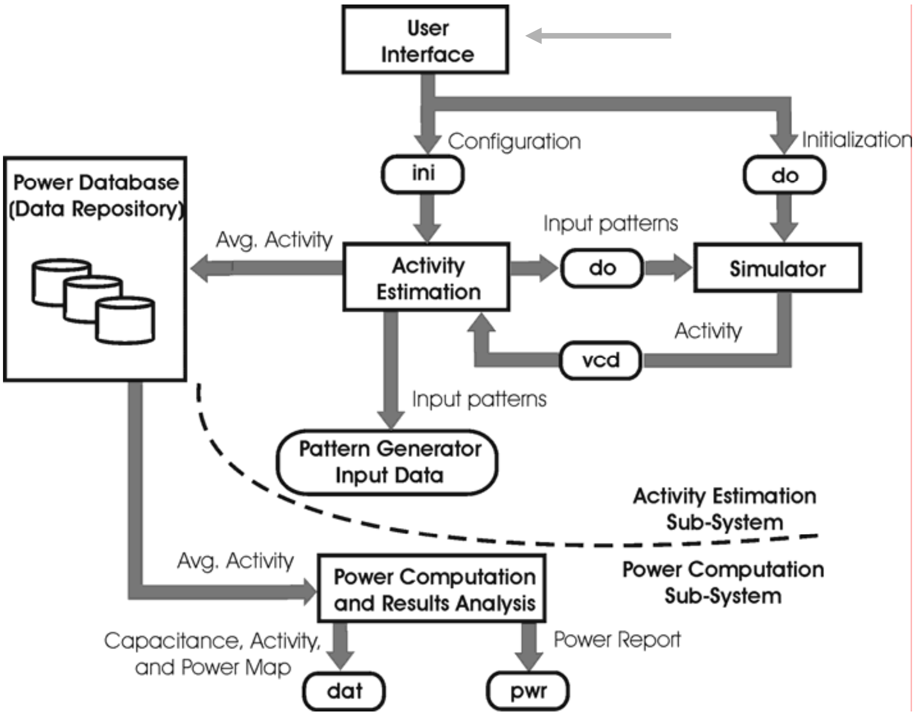
Preparation of the DUT

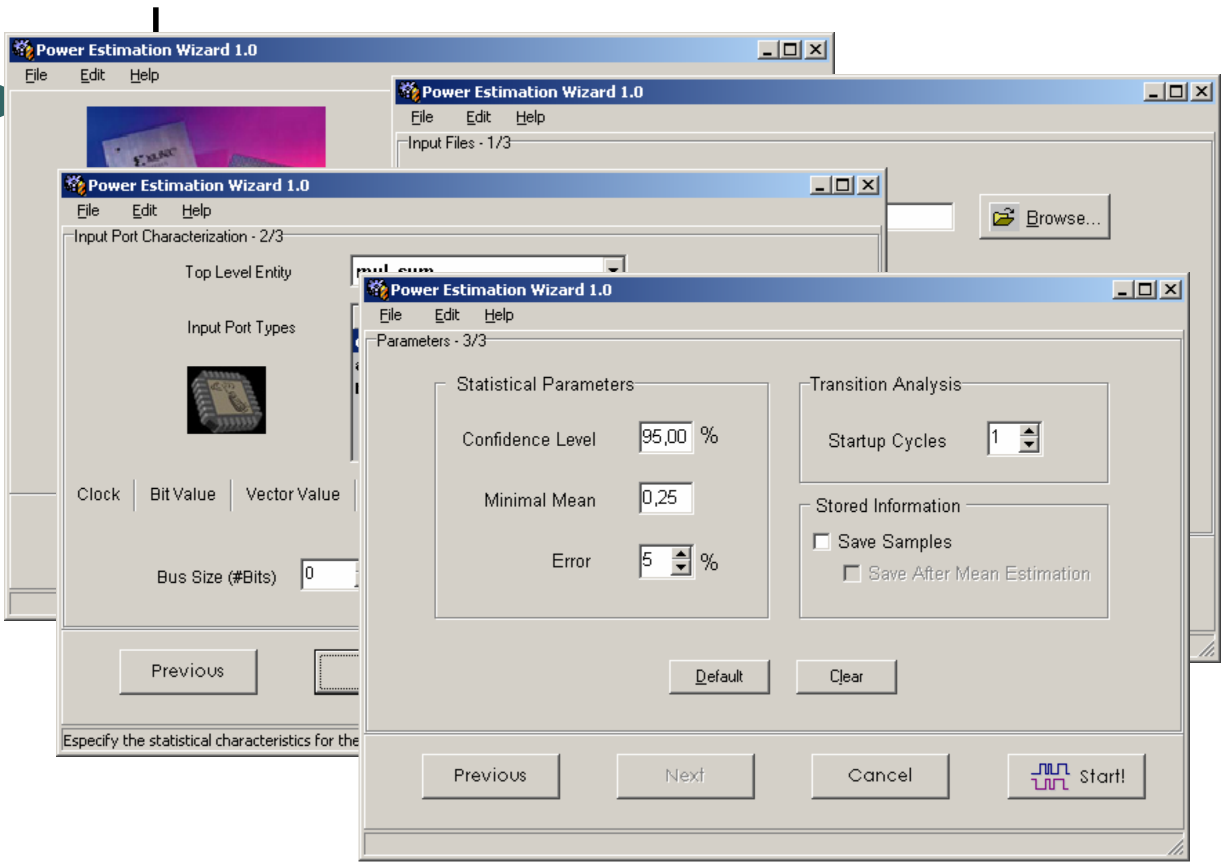
- Synthesis and Implementation
  - *ncd* File (FPGA layout, Xilinx proprietary file)
- netgen (ngdanno, ngd2vhdl in previous versions)
  - VHDL post place and route simulation model
  - *sdf* file (*IEEE P1497 SDF Standard Delay Format for the Electronic Design Process*).

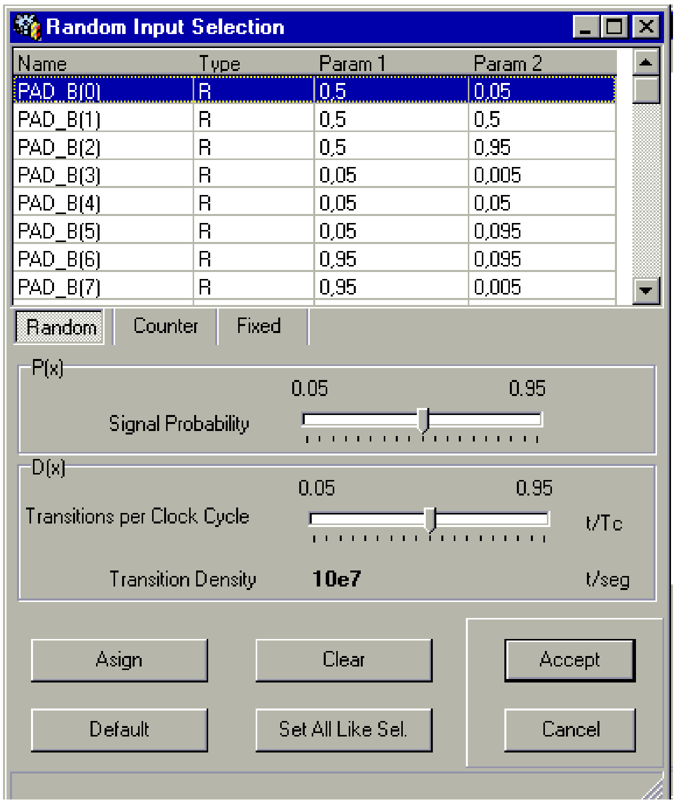
Preparation of the DUT



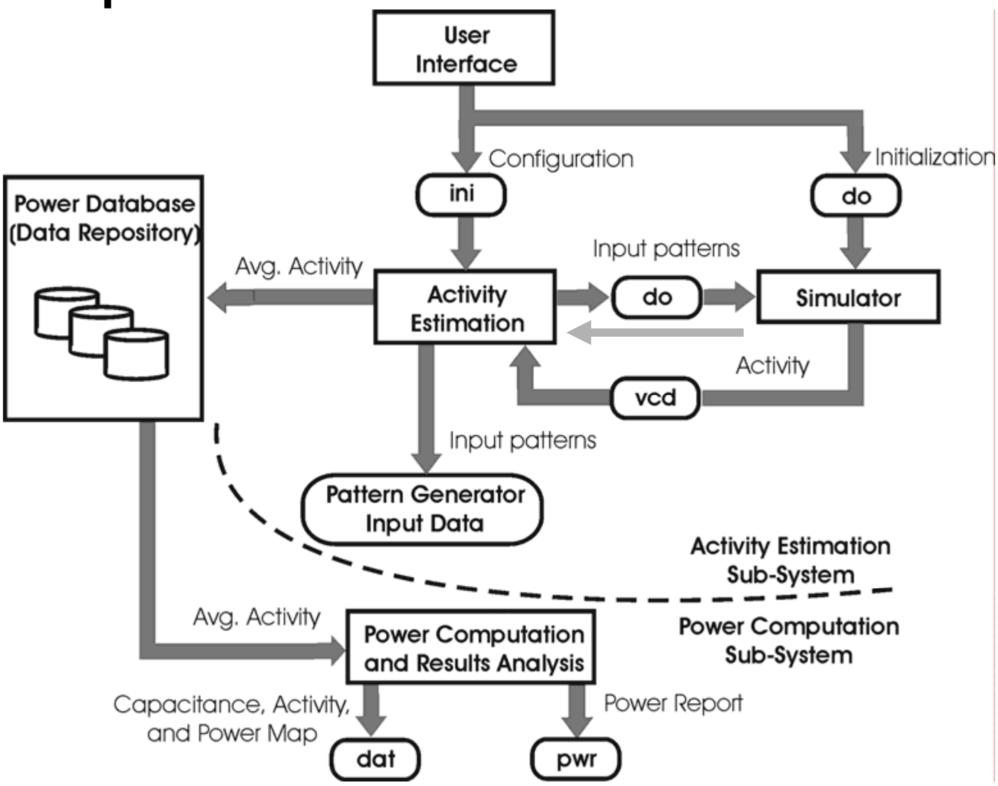
Implementation





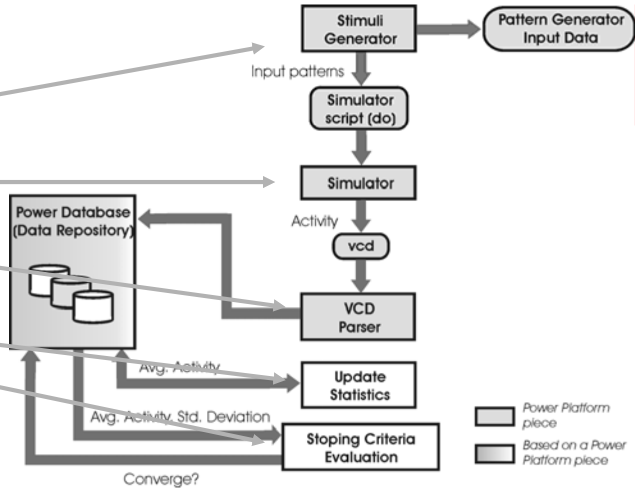


Implementation



Implementation

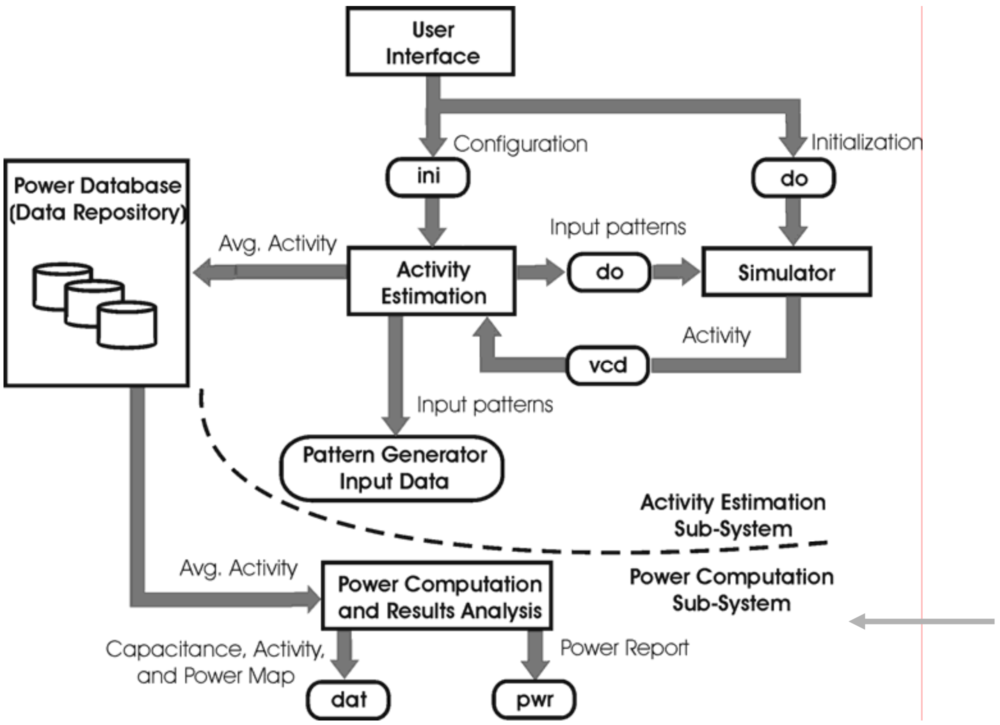
```
# Tcl Code (simplified)
proc transitions {} {
  set END_SIM False
  while { $END_SIM == False } {
    exec generator.exe -pg tla
    do simulate.do
    saveVec
    catch "exec Transitions.exe trans.vcd" Samples
    exec Update.exe
    catch { exec Cuter.exe } END_SIM
   }
   quit –sim
}
```



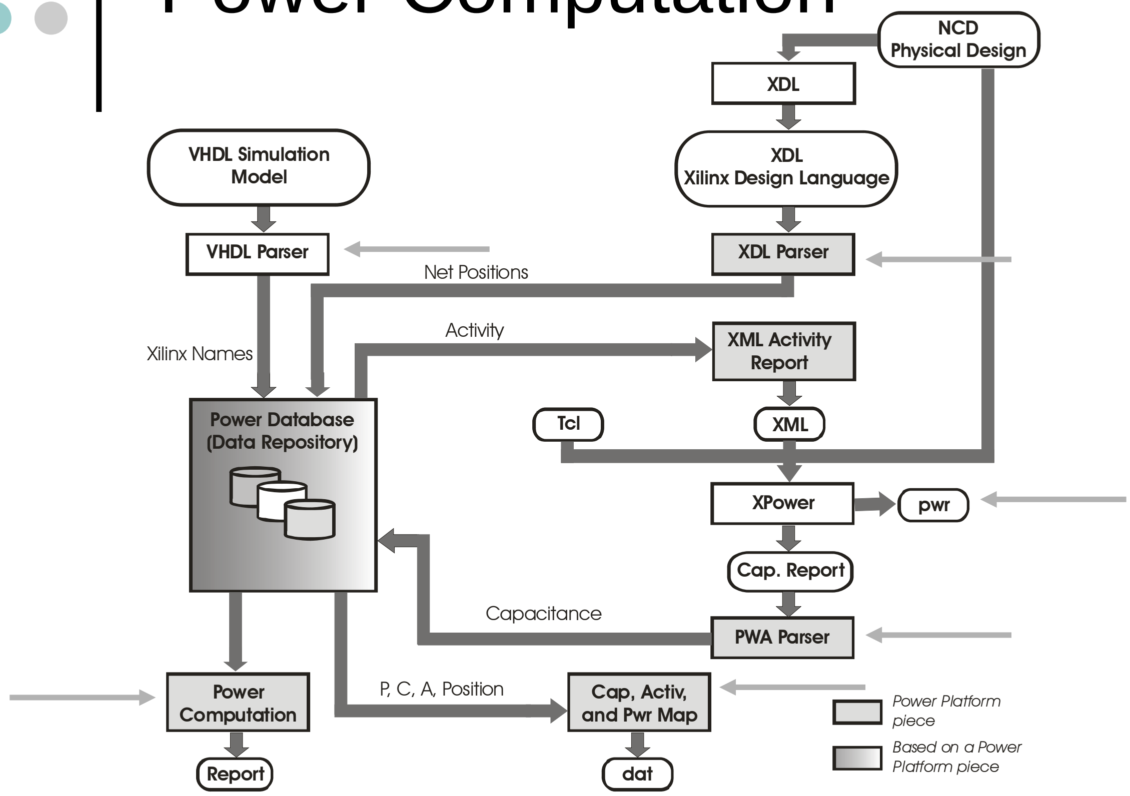
Implementation

- Simulator output format and activity analysis:
  - *vcd* Format (*Value Change Dump*): IEEE p1364-2001, IEEE Standard Hardware Description Language Based on the Verilog® Hardware Description Language.
  - Supported by commercial simulators: ActiveHDL, Modelsim, GHDL…
  - Activity is analyzed by a vcd parser developed in this work.

Power Computation



Power Computation



Test Circuits

Circuit	Code	Description	Device
1	QDDFS- CORDIC(RTL)	Quadrature Direct Digital Frequency Synthesizer based on CORDIC. Portable RTL HDL	XCV300E-8-PQ240
2	QDDFS-CORDIC(RTL-A)	Quadrature Direct Digital Frequency Synthesizer based on CORDIC. Portable RTL HDL with area restriction	XCV300E-8-PQ240
3	FIRDA(1)	Distributed Arithmetic FIR Filter. Completely serial (Digit 1)	XCV400E-8-PQ240
4	FIRDA(2)	Distributed Arithmetic FIR Filter. 2-bit serial (Digit 2)	XCV400E-8-PQ240
5	FIRDA(3)	Distributed Arithmetic FIR Filter. 3-bit serial (Digit 3)	XCV400E-8-PQ240
6	FIRDA(4)	Distributed Arithmetic FIR Filter. 4-bit serial (Digit 4)	XCV400E-8-PQ240
7	FIRDA(8)	Distributed Arithmetic FIR Filter. Completely combinational (Digit 8)	XCV400E-8-PQ240
8	FFT_A	Fast Fourier Transform, version A	XCV800-HQ240-4
9	FFT_B	Fast Fourier Transform, version B	XCV800-HQ240-4
10	FFT_C	Fast Fourier Transform, version C	XCV800-HQ240-4
11	FFT_D	Fast Fourier Transform, version D	XCV800-HQ240-4
12	MULT32-C	Unsigned Combinational 32-bit Multiplier	XCV50PQ240-4
13	ADDER32-C	Unsigned Combinational 32-bit Adder	XCV50PQ240-4
14	MULT16-P	Unsigned Pipelined 16-bit Multiplier	XCV50PQ240-4
15	DIV16-P	Unsigned Pipelined 16-bit Divider	XCV50PQ240-4
16	10MULT16-C	Ten Unsigned Combinational 16-bit Multiplier	XC2V3000FG676-6

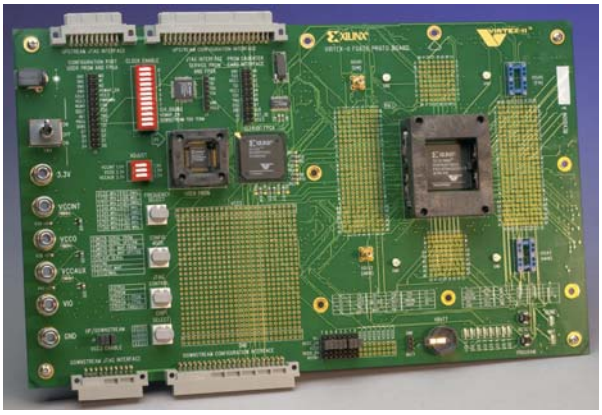
Test Circuits

Circuit	# Slices	Slice FF	#Nodes	Min. Period (ns)
1	484 (15%)	773 (12%)	5411	8.591
2	484 (15%)	773 (12%)	5407	9.220
3	159 (3%)	307 (3%)	1486	5.781
4	303 (6%)	597 (6%)	2774	7.305
5	456 (9%)	897 (9%)	4092	6.276
6	595 (12%)	1177 (12%)	5245	6.484
7	1163 (24%)	2305 (24%)	9495	5.903
8	3424 (36%)	6364 (33%)	32622	12.803
9	3384 (35%)	6364 (33%)	32760	11.767
10	3424 (36%)	6364 (33%)	32242	11.731
11	3424 (36%)	6364 (33%)	32708	10.457
12	640 (83%)	193 (12%)	6627	40.377
13	49 (6%)	97 (6%)	656	11.354
14	172 (22%)	341 (22%)	2194	9.638
15	425 (55%)	831 (54%)	3257	9.899
16	1654 (11%)	586 (2%)	27471	14.928

Test Boards

Xilinx HW-AFX-PQ240-100 development board

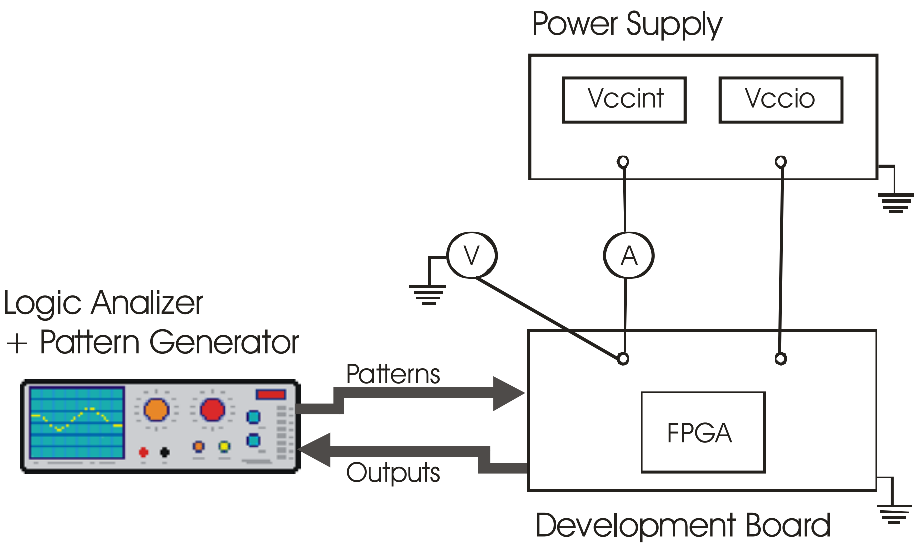
Xilinx Virtex II FG676 development board



FPGAs members used in the experiments

Family	Device	Size (CLB)	Slices	Distributed RAM	BlockRAM
Virtex	XCV50PQ240-4	16x24	768	24,576 bits	32,768 bits
Virtex	XCV800HQ240-4	56x84	9408	301,056 bits	114,688 bits
Virtex-E	XCV300EPQ240-8	32x48	3072	98,304 bits	131,072 bits
Virtex-E	XCV400EPQ240-8	40x60	4800	153,600 bits	163,840 bits
Virtex-II	XC2V3000FG676-6	64x56	14336	448 Kb	1728 Kb

Experimental Setup

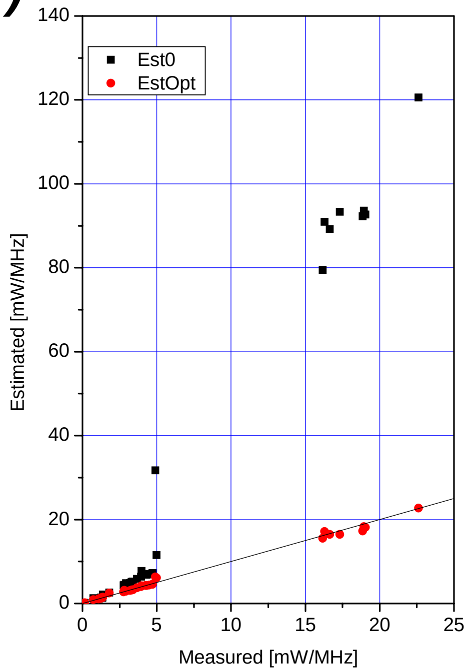


Experimental Results

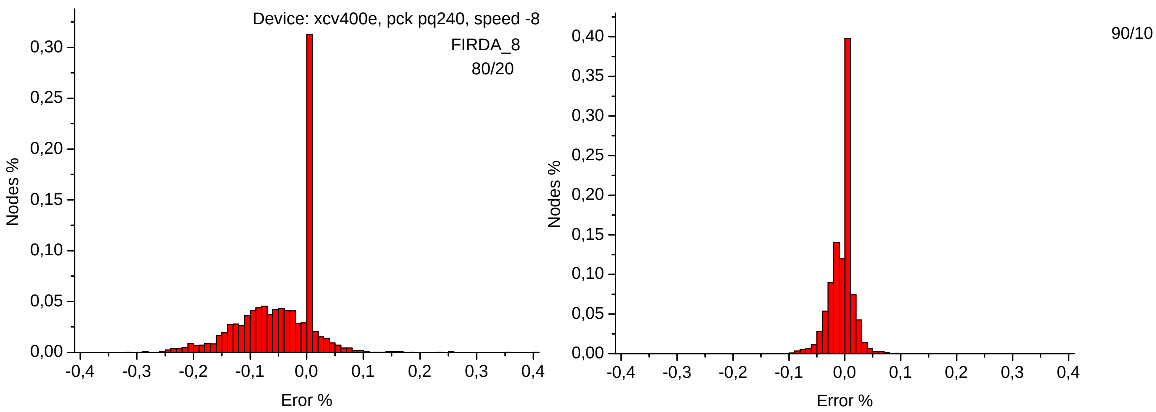
- Total dynamic power estimation
- Individual node power estimation
- Error analysis
- Tunable accuracy-execution time properties
  - Error-Confidence
  - Activity threshold
- Importance of primary input definition
- Power maps
- Energy of the computation

Experimental Results (Total Power)

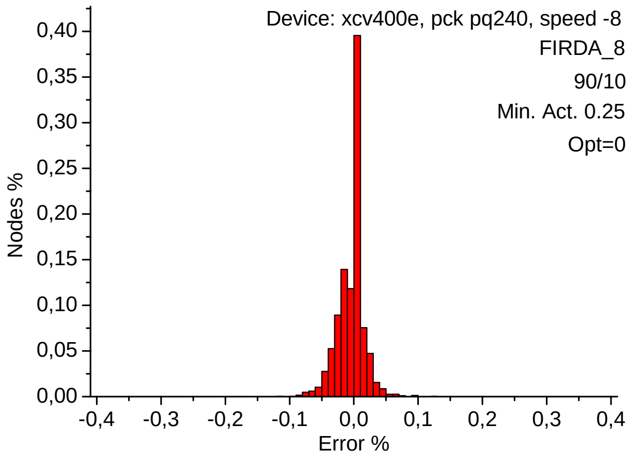
Virtex 50

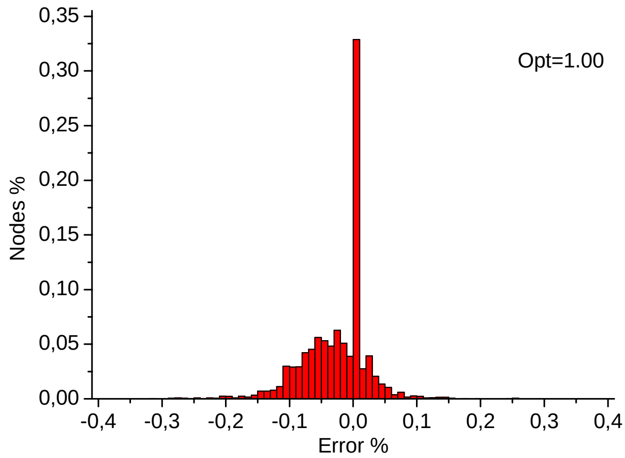


Experimental Results (Individual Power)



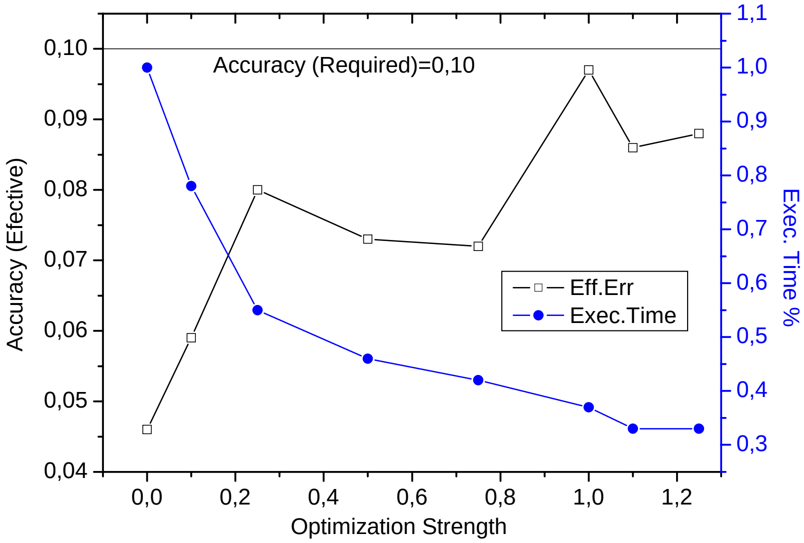
Experimental Results (Individual Power)



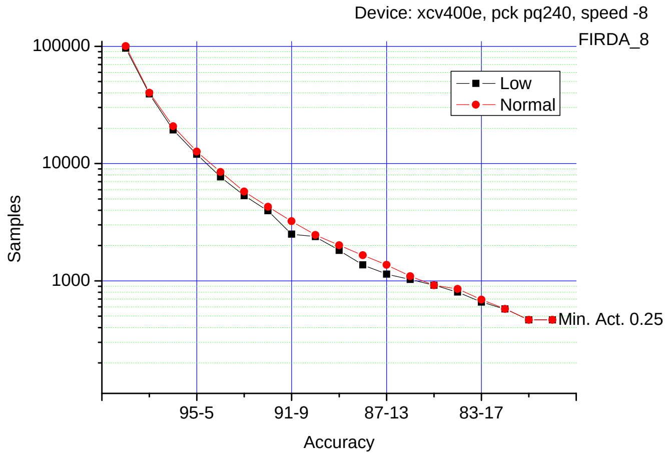


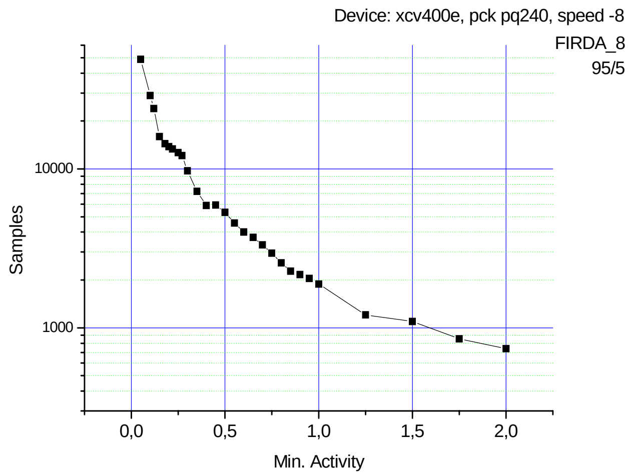
Experimental Results (accuracy vs. optimization)

Device: xcv400e, pck pq240, speed -8 FIRDA_8 90/10

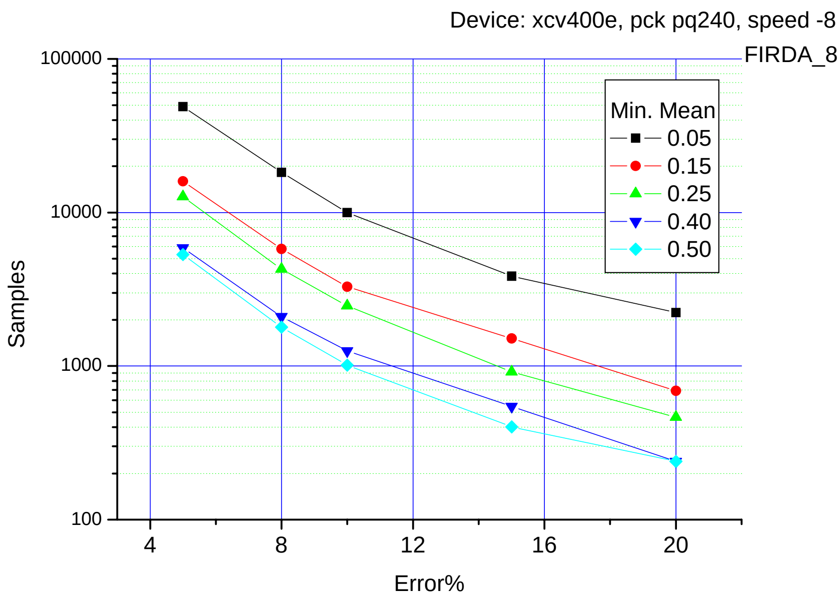


Experimental Results (accuracy vs. exec. time)





Experimental Results (accuracy vs. exec. time)



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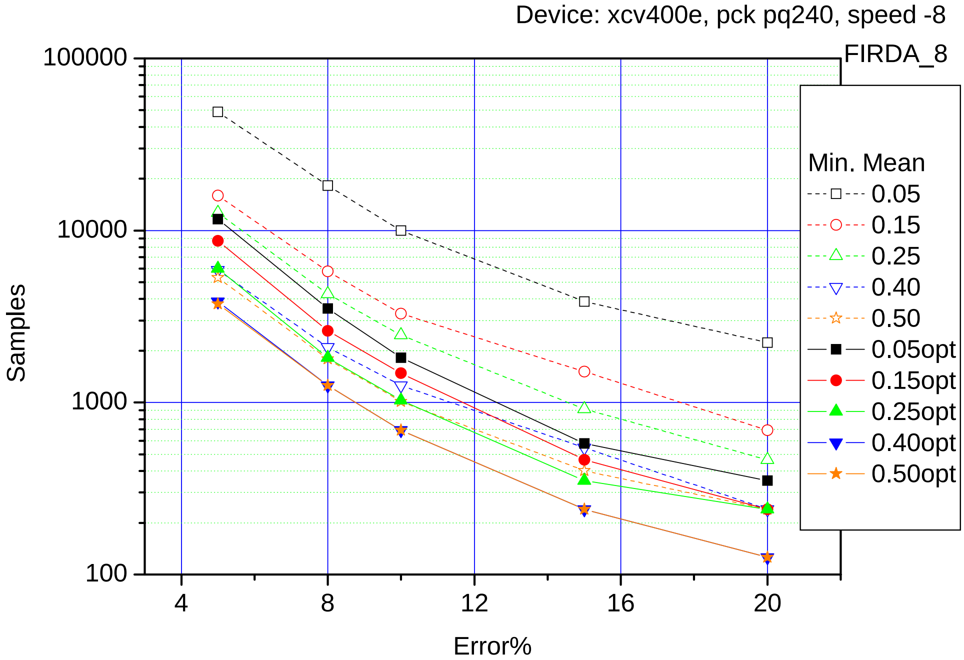
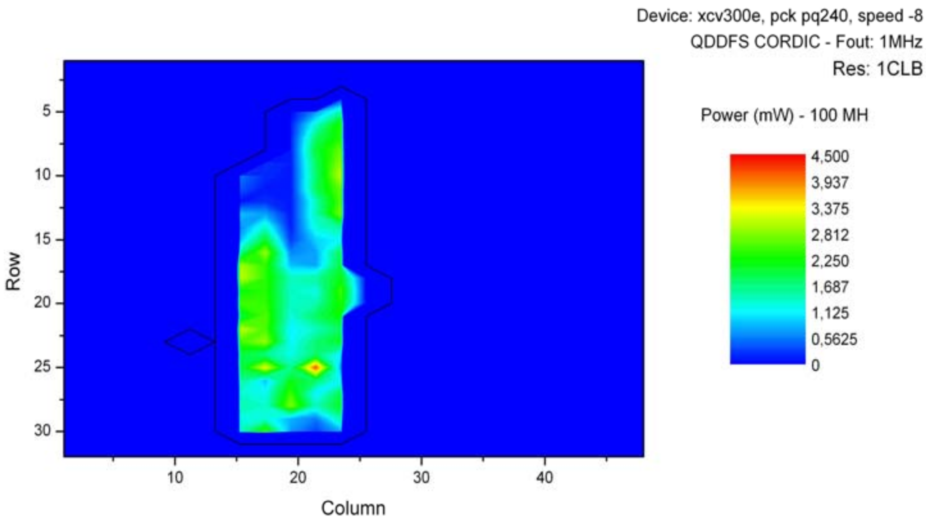


Experimental Results (Power Maps)



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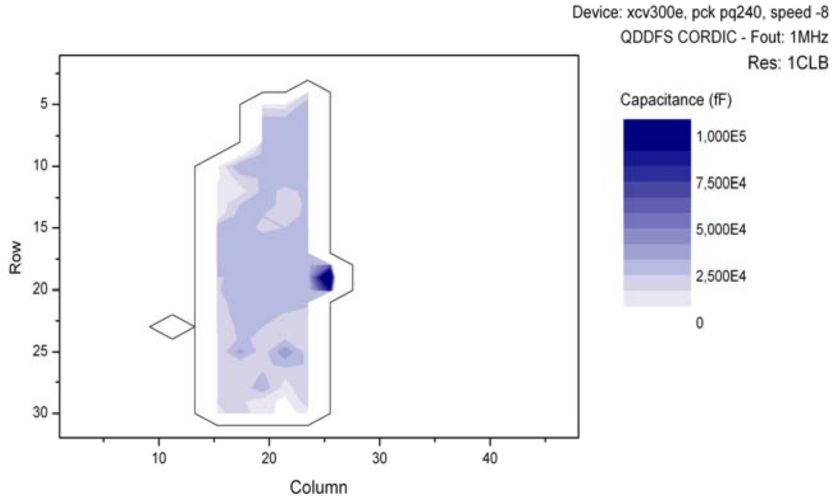

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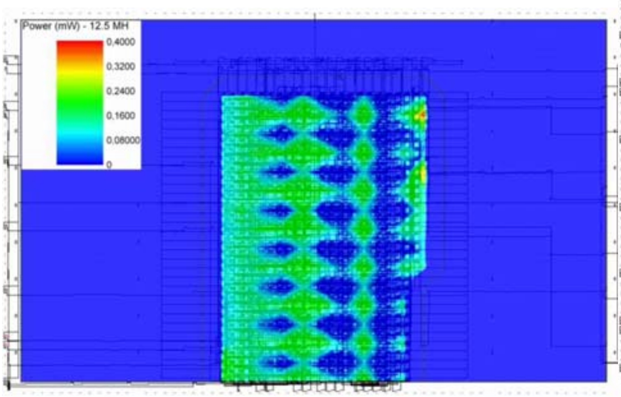
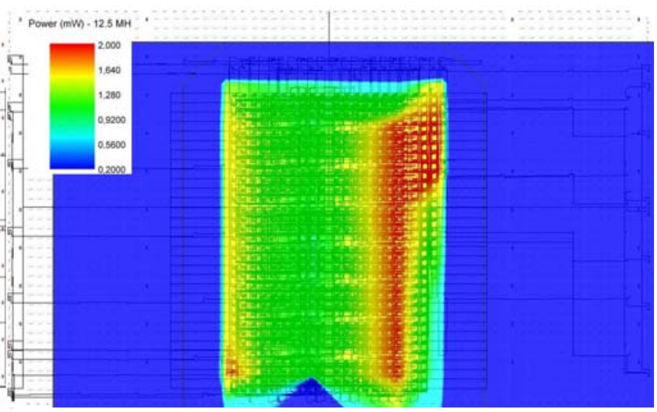
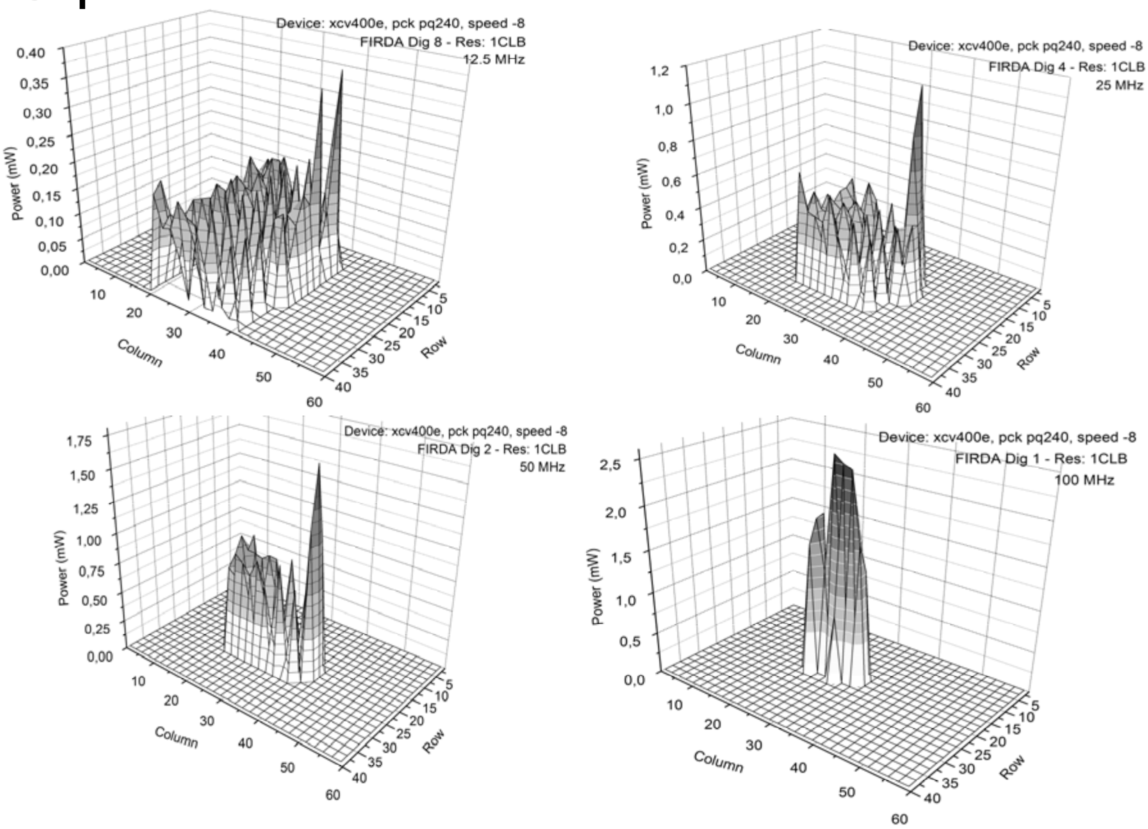
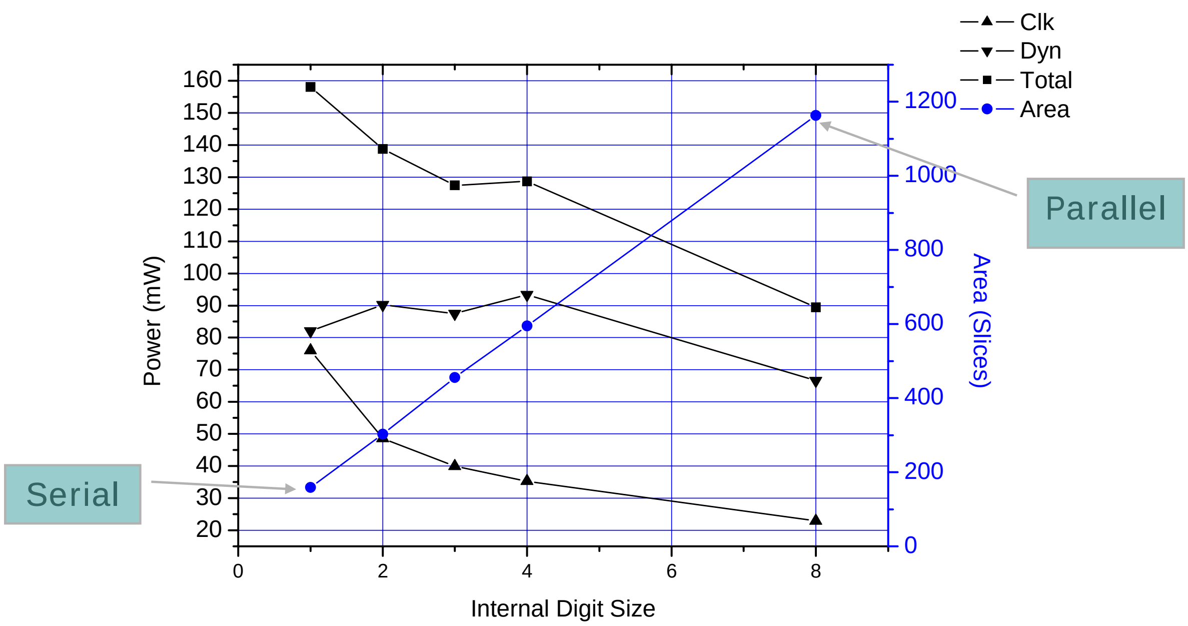




Experimental Results



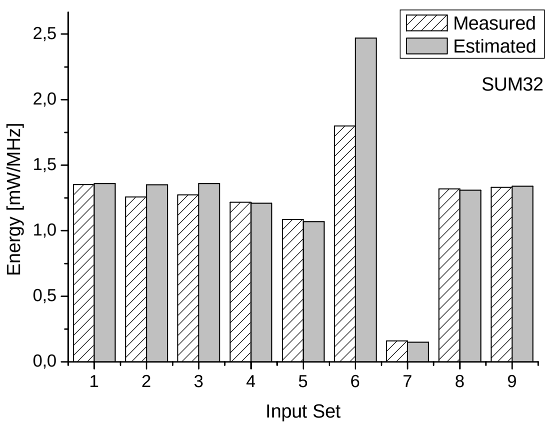
Experimental Results (Energy of the Computation)

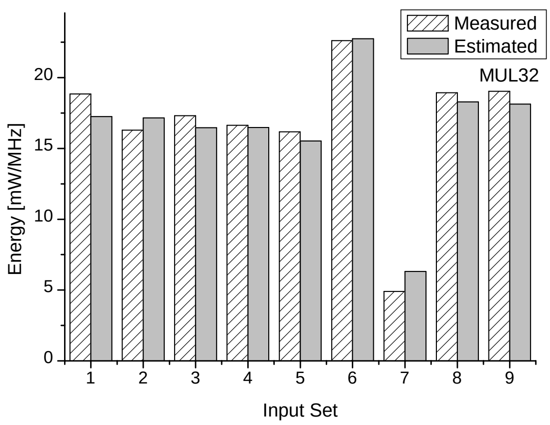


Experimental Results (Impact of the Input Patterns Definition)

Test Case	Description
1	All inputs are independent random patterns
2	The activity for the MSB is set to 0.05 and is increased linearly to 0.95 for the LSB.
3	The activity for the MSB is set to 0.95 and is decreased linearly to 0.05 for the LSB.
4	The activity is set to 0.05 for the 4 MSBs and 0.5 for the rest.
5	The activity is set to 0.05 for the 8 MSBs and 0.5 for the rest.
6	The activity is set to 0.95 for all the bits.
7	The signal probability is set to 0.95 for all the bits.
8	The 4 LSBs are connected to a counter and the rest are independent random bits.
9	The 4 MSBs are connected to a counter and the rest are independent random bits.

Experimental Results (Impact of the Input Patterns Definition)





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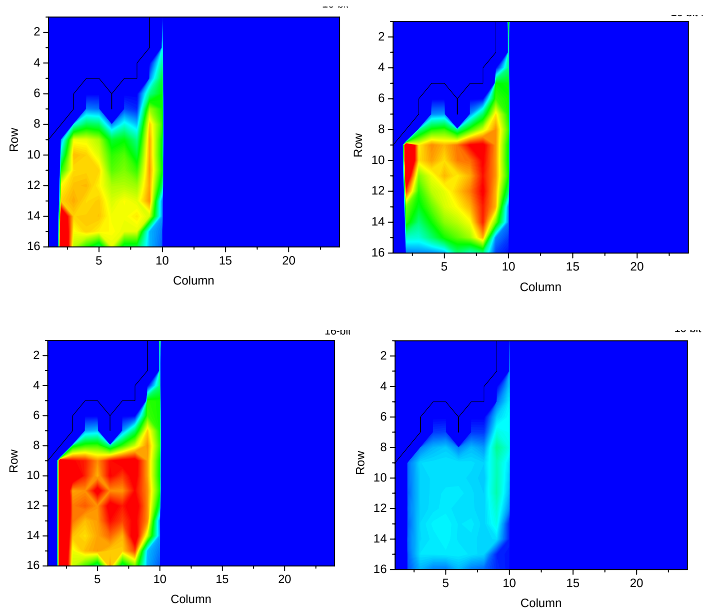


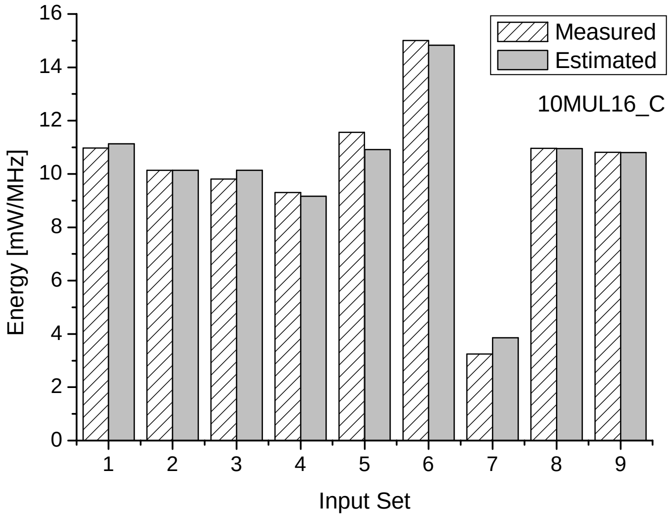
Additional Experiments on Virtex-II

Impact of the Input Patter Definition on Total Power

Case	Measured	Tg = 50		Opt. Tg	
		Estimated	Error (%)	Estimated	Error (%)
1	10.97	43.92	300.7	11.13	1.6
2	10.14	42,30	317.3	10.14	0.0
3	9.81	39.90	306.7	10.14	3.3
4	9.31	36.57	292.7	9.17	-1.5
5	11.56	41.22	256.5	10.92	-5.6
6	15.01	62.09	313.6	14.83	-1.2
7	3.25	14.77	354.2	3.86	18.8
8	10.96	45.26	312.8	10.95	-0.1
9	10.81	43.88	305.9	10.80	-0.1

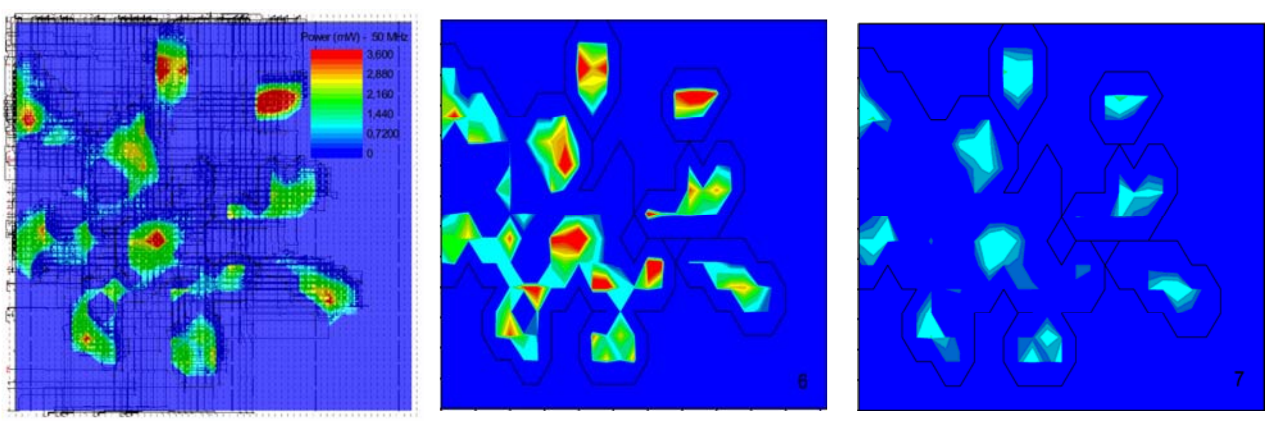
Additional Experiments on Virtex-II

Impact of the Input Patter Definition on Total Power



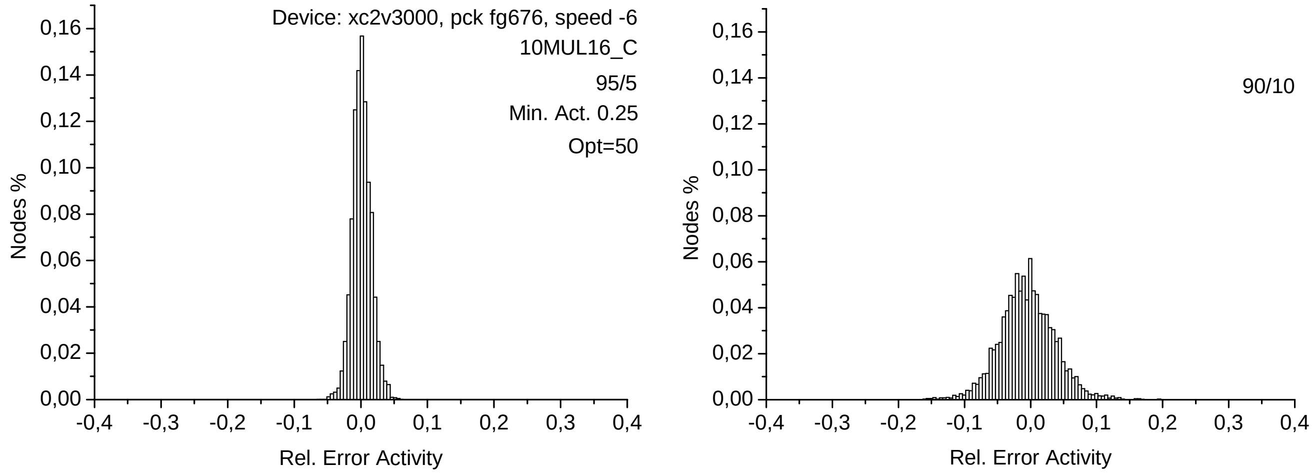
Additional Experiments on Virtex-II

Impact of the Input Patter Definition on Total Power



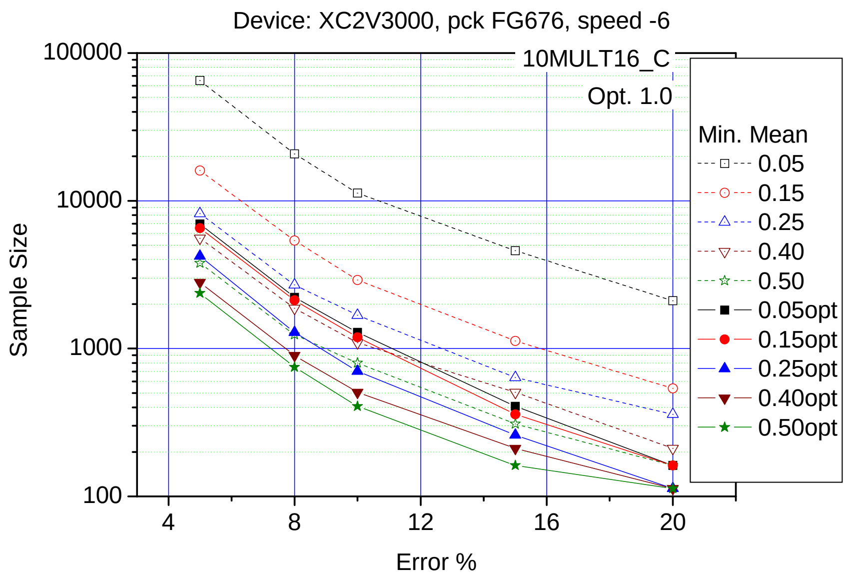
Additional Experiments on Virtex-II

Dynamic Power Estimation for Individual Nodes



Additional Experiments on Virtex-II

Accuracy vs. Execution Time Tradeoff



Additional Experiments on Virtex-II

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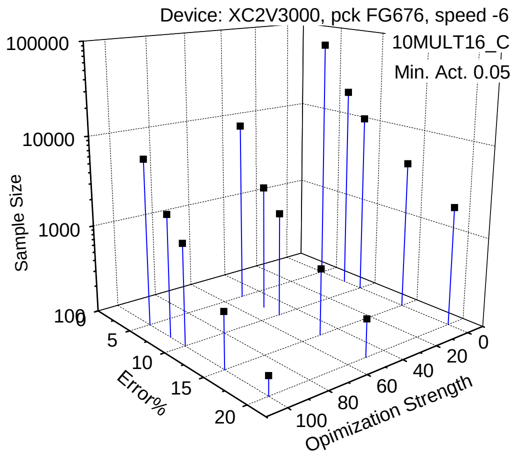
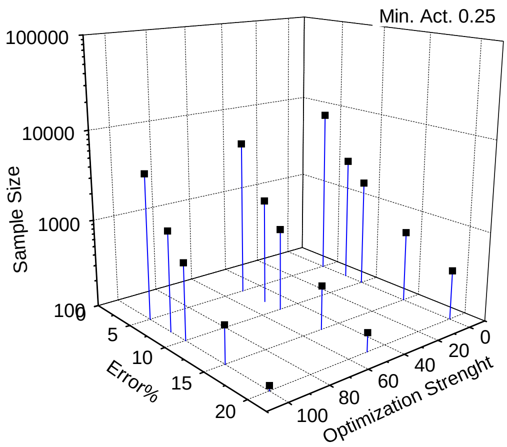
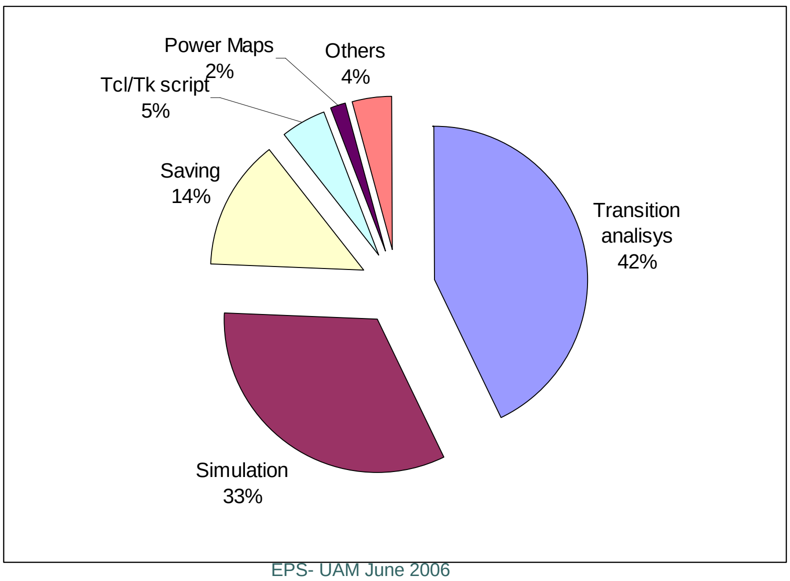




Additional Experiments on Virtex-II

Evaluation of the EDA Tool



Main Contributions and Conclusions

- Applicability of statistic-based techniques in the FPGA design environment.
  - A-B Nodes Classification
  - Power Platform
  - A-DyP
- Short-pulse Filtering as a Calibration Resource
- Robustness of the statistical approach : Tunable accuracy
  - Error-confidence
  - Min. Mean
  - Optimization Strength
- Bounded relative error for individual nodes.

Main Contributions and Conclusions

- Importance of the input pattern characterization.
- Use of standard formats widely accepted in the industry.
- Design Automation.
- Power, Capacitance and Activity Maps
  - Hot Spots
  - Diagnose
  - Power optimization
- Energy of the Computation

Publications

- 20 publications related with this thesis. The most important are:
  - E. Todorovich and E. Boemo, “A-B Nodes Classification for Power Estimation”, 16th International Conference on Field Programmable Logic and Applications (FPL 2006), August 28-30, Madrid, Spain.
  - E. Todorovich, F. Angarita, E. Boemo, “Statistical Power Estimation for Fpga’s”, 15th International Conference on Field Programmable Logic and Applications (FPL 2005), pp. 515-518, ISBN: 0-7803-9362-7, August 24-26, Tampere, Finland.
  - E. Todorovich, E. Boemo, F. Cardells, J. Valls, “Power Analysis and Estimation Tool integrated with XPower”, Twelfth ACM International Symposium on Field-Programmable Gate Arrays, FPGA 2004, Monterey, California, USA, February 22-24, 2004. ISBN 1-58113-829-6.
  - E. Todorovich, M. Gilabert, G. Sutter, S. Lopez-Buedo, and E. Boemo, “A Tool for Activity Estimation in FPGAs”, Lecture Notes in Computer Science, Vol. 2438, pp. 340-349. Springer-Verlag, Berlin Heidelberg 2002.
  - G. Sutter, E. Todorovich, S. Lopez-Buedo, E. Boemo, “Low-Power FSMs in FPGA: Encoding Alternatives”, Lecture Notes in Computer Science, Vol. 2451, pp. 363-370. Springer-Verlag, Berlin Heidelberg 2002.
  - G. Sutter, E. Todorovich, S. Lopez-Buedo, and E. Boemo, "FSM Decomposition for Low Power in FPGA", Lecture Notes in Computer Science, Vol. 2438, pp. 350-359. Springer-Verlag, Berlin Heidelberg 2002.

Future Works

- Testing A-DyP on other Xilinx FPGA technologies
- Porting A-DyP to Altera FPGAs
- Other statistics-based power estimation methods
  - Total power estimation for big sequential circuits,
  - Advanced sampling techniques for hierarchical designs, etc.
- Peak or maximum power estimation
- Static Power optimization
- Early capacitance estimation
- EDA tools for Low Power Design
- Temperature Estimation

Future Works

- High-level Power Estimation
  - Hard core power estimation
  - High-level power estimation based on neural networks
  - IP power characterization
  - Power Estimation for embedded processors
  - Impact of RTL synthesis

Statistical Power Estimation on FPGAs

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