Clock Gating and Clock Enable for FPGA Power Reduction

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Abstract—**This paper presents experimental measurements of power consumption using different techniques to turn off part of a system and switch between active and standby modes. The main ideas analyzed are: clock gating, clock enable, and blocking inputs. The laboratory work is described, including the measurement setups and the benchmark circuits. Quantitative measurements in both a 65 nm CMOS Cyclone III and a 45 nm CMOS Spartan 6 FPGAs are presented. The selected circuits used as benchmarks are different type of multipliers. Results of power consumption in active and standby modes are presented and compared.**

Keywords-low-power; clock-gating; clock-enable; power measurements

I. INTRODUCTION

Since first introduced in the mid-80s, the focus of research on FPGA architecture and CAD tools has been centered on improving area and speed. But, in recent years, with the growth of portable applications, there has been an increasing interest in power efficiency.

One of the simplest ideas to reduce dynamic power is to temporarily turn off the inactive parts of a system, or put unused modules into a standby mode. This can be done in different ways: turning off the power supply, disabling the clock, or blocking the inputs.

Several of these techniques are widely used in the ASICs world, but in FPGAs they are limited to the available resources. Some FPGAs incorporate suspend or hibernate modes [1][2], but these modes are applied to the whole chip and do not allow partial utilization.

Modern FPGAs also include several clock control blocks that allow to shutting-down the clock line in some parts of the circuit. For example, the Xilinx devices since Virtex II, II Pro and Spartan-3; or Altera since from Cyclone II and Stratix II.

If a designer wants to optimize the power of a SoC in an FPGA design the questions to be answered are: “What are the alternatives to shut down parts of the system?” and “What are the pros and cons of each one?”

The main purpose of this work is to analyze and compare three different techniques available in FPGAs to temporarily disable blocks. The studied ideas are: clock gating, clock enable and blocking the inputs. Comparisons are based on experimental measurements of power consumption.

For clock gating, we used only the available clock control signals, because doing clock gating inserting a logic elements in the clock tree is not recommended due to the additional skew and the difficulty in generating a glitch-free signal. This limits the possibilities of making a fine grain control, because the chip only has a few clock control blocks. But, on the other hand this type of clock gating appears to be a priori the best alternative, since it reduces the power consumption in flip-flops and the clock network.

The second studied technique is simpler, and consists in using the clock enable (CE) input of the FF. This brings no time constraints, and allows shutdown of blocks in fine grain, but a priori it is not too effective. It just turns off the FF consumption and the logic, but it does not reduce the power of the clock tree.

The third technique is based on disabling the datapath, by blocking the inputs. This can be done in several ways, but in this paper, we tested a FF barrier. As the previous case, the logic and the FFs maintain their values with the corresponding power reduction, but the clock network is still active.

The work emphasize on on-board measurements and quantitative results of applying these three techniques on an Altera Cyclone III and a Xilinx Spartan 6. As benchmark blocks we use different type of multipliers. A linear feedback shift register (LFSR) is employed to generate pseudo-random inputs, and a parity function was selected to get a unique output. Thus, the obtained measurements corresponds to the core of the FPGAs.

The remainder of the paper is organized as follows: Section II describes related work on clock gating for power reduction in FPGAs. Section III describes the measurement setups and the experimental work. The obtained results are presented in Section IV. Finally conclusions and suggestions for future work appear in Section V.

This work was partially funded by the Uruguayan Agency for Research and Innovation (ANII) under grant PR-POS-2008-003 and the "2011 Latin American Research Project Banco Santander-UAM" funding initiative. Additional resources have been obtained from CICYT Project TEC2007-68074-C02-02/MIC.

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II. RELATED WORKS

There is a large volume of published studies describing the role of clock gating as a low power technique in ASICs, most examples were published in the decade of 1990 [3][4][5]. Then, the technique are incorporated in several EDA tools that are capable of generating automatic clock gating from an HDL description [6][7][8][9]. Recently, the ideas have been extended to FPGAs in [10].

There are some works that specifically studied the use of clock gating in FPGAs to reduce power: [11] evaluates the performance of gated clocks for a specific pipelined Cordic core in Xilinx FPGAs. The use of clock gating and different blocking techniques to select between two different data paths are presented in [12] and [13]. Reference [14] analyze the clock-gating technique in FPGAs for a set of design cases, comparing both the FPGA and ASIC results. [15] consider and evaluate FPGA clock network architectures with built-in clock gating capability. Finally [16] proposes a reconfigurable clock-gating technique.

Our work contribute to the previous research line by presenting quantitative measurements in both, a 65 nm CMOS Cyclone III, and a 45 nm CMOS Spartan 6 FPGAs, comparing active and standby modes with three different techniques. Also we provide a LPD guidance applicable to FPGA-based SoC, where is possible to put in standby mode some parts of the circuit.

III. EXPERIMENTAL WORK

A circuit with two blocks was developed in order to design the experiments (Fig. 1). One block is the circuit under test: unsigned integer multipliers with latched inputs and outputs. The other block embrace the on-chip test vector generator, composed by a digital clock manager (DCM) and a linear feedback shift register (LFSR).

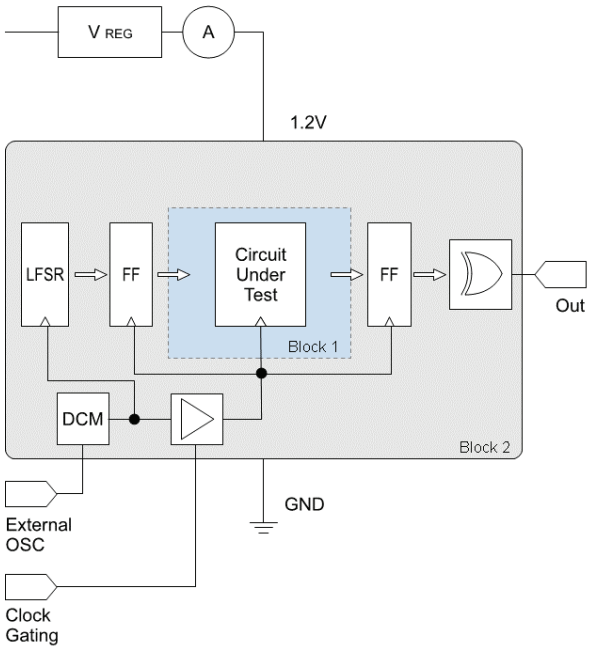

Figure 1. Experimental Clock Gating Setup

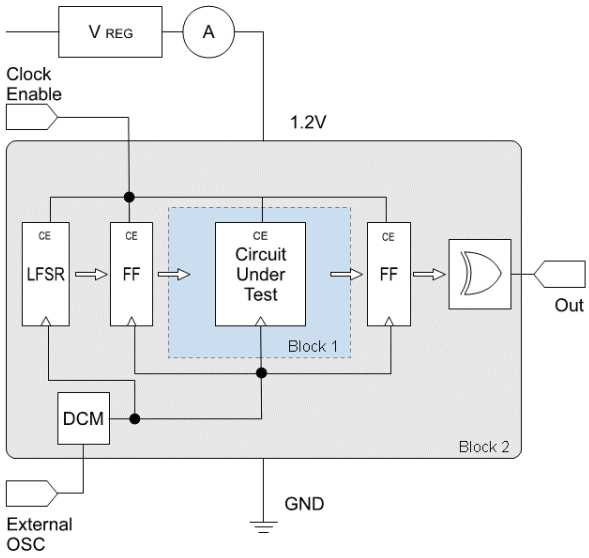

Figure 2. Experimental Clock Enable setup.

The LFSR output, a variable pseudo-random signal, was connected to the input of the multipliers to test all possible combination. The outputs of the multiplier were combined in a multi-input exclusive-or gate, or a parity generator, and feeded the result to a unique output pin (this output is necessary only for the proper synthesis of the circuit). This experimental setup minimizes the use of inputs and outputs and its influence in the design [17] and [18].

The block with the LFSR and the DCM was common to all experiments while the second block was modified for the different experiments. In some cases, a single multiplier was used and the number of pipeline stages was varied, while in others, the variation was made by changing the number of multipliers (Table I). These scenarios were created to compare the power consumption reduction for each technique.

Two different manufacturers' boards were used to perform the measurements. Each board required a different setup to measure power consumption. Even though the external oscillators of the Xilinx and Altera boards have different frequencies, all experiments were performed with an internal fixed clock frequency of 50MHz generated by the DCM block.

TABLE I. DESIGN DESCRIPTIONS

Design	Design Descriptions	
	Number of Multipliers 32x32	*Pipelines per Multipliers*
M_1	1	0
M_2	1	1
M_3	1	3
M_4	1	5
M_5	2	5
M_6	3	5

Three techniques were used to switch between active and standby operations mode, and the implementation of each one required small variations of the circuits.

The first technique is clock gating (Fig. 1). To implement clock gating inside a FPGAs is necessary to employ the appropriate clock control block provided by the manufacturer. In the case of Altera devices, it is possible to generate a global clock with enable port using the megafunction ALTCLKCTRL [19]. In the case of Xilinx devices the BUFGCE primitive makes possible the function of clock enable [20]. This primitive is built from the BUFGMUX, a glitch-free clock multiplexer, maintaining a fixed value for one input if clock that entre for the other input is disabled.

The second technique is the use of the clock enable input that is present in all the flip-flops inside the FPGAs (Fig. 2). When the CE signal is disabled, the block enters in standby mode.

The third technique consisted in blocking the datapath in order to maintain the inputs of the multipliers in a constant value. This is made deactivating the CE input in the flip-flops that latches the multiplier inputs. In this case, in order to avoid data dependency a large number random of constant values was used, and the final value was the average of all the measured power consumption.

A. Cyclone-III Measurement Setup

The measurements were performed using a Terasic DE0 board, with an Altera Cyclone III 3C16 FPGA device. This board is not specifically designed to perform power measurements, therefore some modifications were made in order to measure the internal core power consumption (the IO power value is practically independent of the technology and was not measured). The on-board 1.2 Volts regulator was removed and substituted by a circuit that includes an external regulator and a serial shunt. The average power consumption measurements were performed using a Fluke 45 multimeter.

B. Spartan-6 Measurement Setup

The measurements on this board were performed using a Xilinx Spartan-6 LX16 Evaluation Kit.

Spartan has a Cypress PSOC which allows the designer to obtain a direct measure of current in all FPGA power lines by sensing the voltage in a shunt resistor. To use this feature, a set of Matlab tools was developed. These tools queried the PSOC via USB and collected a set of measures all at once.

The power consumption was determined by sensing the core power line voltage (1.2 V) and averaging 500 measures for two identical boards. The system was calibrated with a Fluke 45 multimeter to get comparable results.

IV. RESULTS

Three previous techniques of clock gating were applied in different size circuits. For each circuit version, two activity states were measured: standby and active.

The power consumption of the DCM, the LFSR, and the parity generator was separate measured and then subtracted to the total power measured; then data in Table II and III only show the consumption of the circuits under test.

A. Standby power consumption

Turning off all the clock lines with clock gating resulted in a standby consumption that is practically independent from the circuit size. Therefore, the power consumption reduction for this technique is maximum.

The results obtained with the clock enable technique show that power is significantly reduced with respect to active mode, but is greater than the previous case. This result was expected because - in this case - the clock network is always active.

Another remarkable result of the clock enable technique is the strong linearity between standby power and the number of flip-flops of the design; as can be seen in Fig. 3 and Fig. 4.

Theoretically, using blocked inputs technique the standby power consumption should be comparable to the power consumption of clock enable. In practice, this was observed in Xilinx (Fig. 3). However, in Altera devices (Fig. 4), standby consumption for blocked inputs was greater than the consumption for clock enable.

TABLE II. POWER CONSUMPTION SPARTAN-6

Design	**Number of FF**	**Active Consumption @50MHz (mW)**			**Standby Consumption (mW)**		
		Clock Gating	***Clock Enable***	***Blocked Inputs***	***Clock Gating***	***Clock Enable***	***Blocked Inputs***
M_1	192	46.0	44.3	50.2	0.2	1.1	1.5
M_2	256	43.5	45.2	47.3	0.1	1.5	1.3
M_3	947	28.2	27.1	26.4	0.1	3.6	3.5
M_4	1285	27.3	26.4	26.3	0.1	4.6	4.4
M_5	2442	54.0	55.1	40.2	0.2	8.7	8.9
M_6	3657	95.8	121.8	110.8	0.3	11.6	12.1

TABLE III. POWER CONSUMPTION CYCLONE III

Design	**Number of FF**	**Active Consumption @50MHz (mW)**			**Standby Consumption (mW)**		
		Clock Gating	***Clock Enable***	***Blocked Inputs***	***Clock Gating***	***Clock Enable***	***Blocked Inputs***
M_1	192	43.1	40.3	39.5	0.1	1.2	1.4
M_2	614	32.1	30.2	30.0	0.1	1.4	3.3
M_3	1086	29.0	28.7	27.2	0.1	2.1	4.1
M_4	1525	34.4	30.9	32.0	0.2	2.3	9.0
M_5	2915	64.4	57.7	62.2	0.3	3.6	15.5
M_6	4271	94.8	86.9	90.9	0.5	5.4	22.5

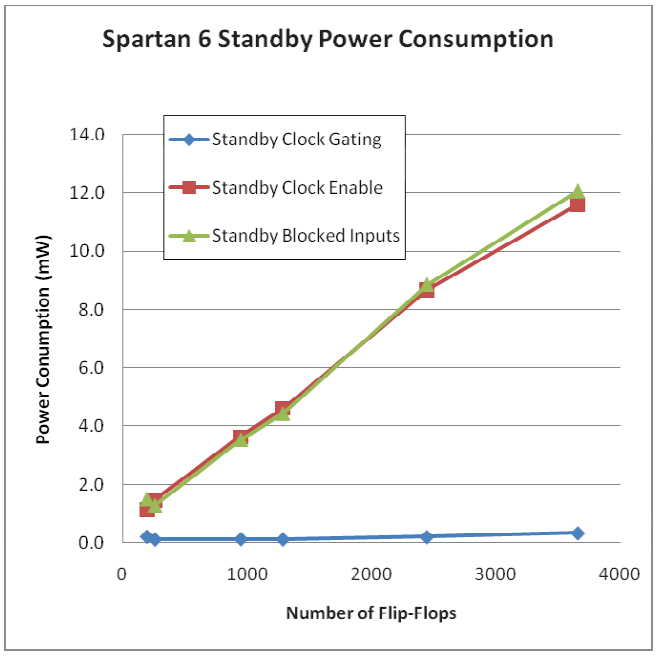

Figure 3. Spartan 6 Standby power consumption vs. Number of FF

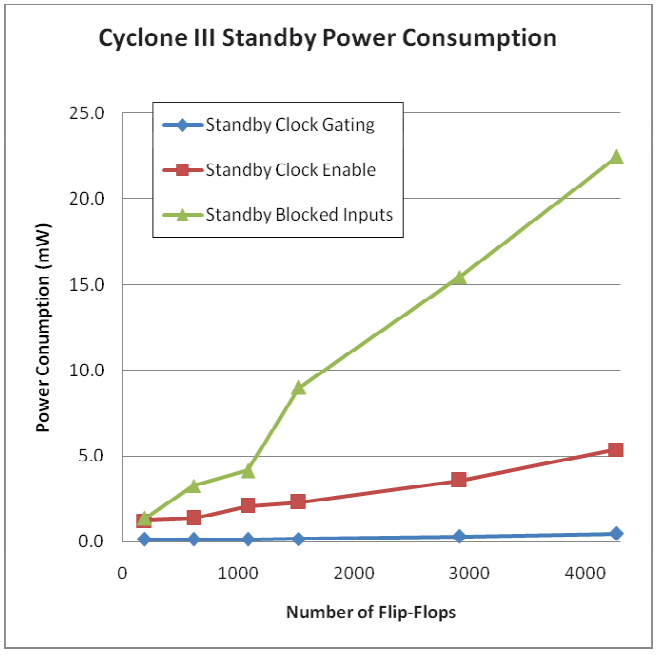

Figure 4. Cyclone III Standby power consumption vs. Number of FF

B. Active power consumption

The most remarkable result was that in the three cases the power consumption was almost the same in active mode. It can be observed in Fig. 5, that for Xilinx this is true in most cases except for the design M_6 where the differences are significant. For this design CE is the option that consumed more power and CG is which consumed the less one.

The Fig. 6 illustrates a slightly different result for the Altera device. In this case CG is the option with more power consumption and CE is the option with the less one.

It also can be observed from Fig. 5 and Fig. 6 the well-known result that adding pipeline stages reduces power consumption [21].

V. CONCLUSION

In this paper, we considered three techniques to turn off part of a system and switch between active and standby mode, the techniques are: clock gating, clock enable and blocking inputs.

The first conclusion is that turning off part of the system in any of the three studied techniques always improve the power figure. The best option is to use global clock gating. The most interesting feature of this technique is that the power is almost independent of the circuit size. The use of multiple global clock networks is not easy and has several design problems, but in the case of SoC with large blocks, when it is possible to work in coarse-grain, this is the best option.

The use of CE is a good option when the design does not have a large amount of flip-flops. In this case, the consumption of this option is very linear with the number of flip-flops. The technique is very simple, does not have timing problems, and is useful in fine grained designs.

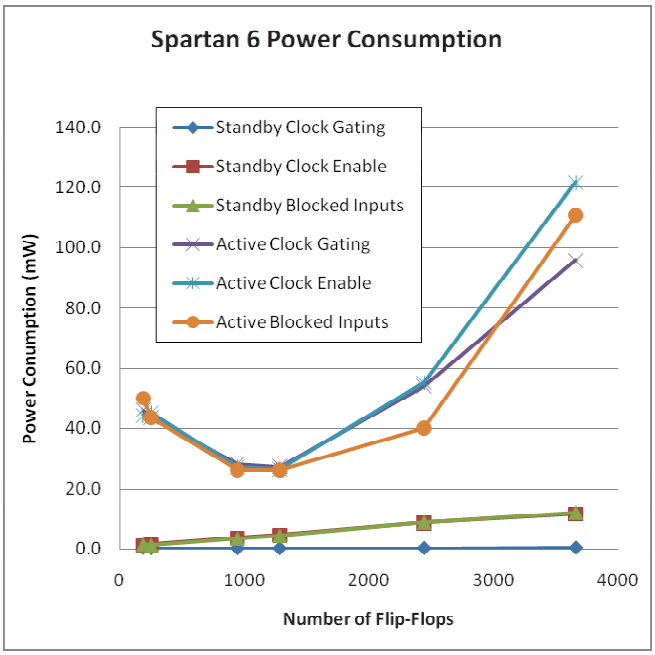

Figure 5. Spartan 6 Standby and Active power consumption vs. Number of FF

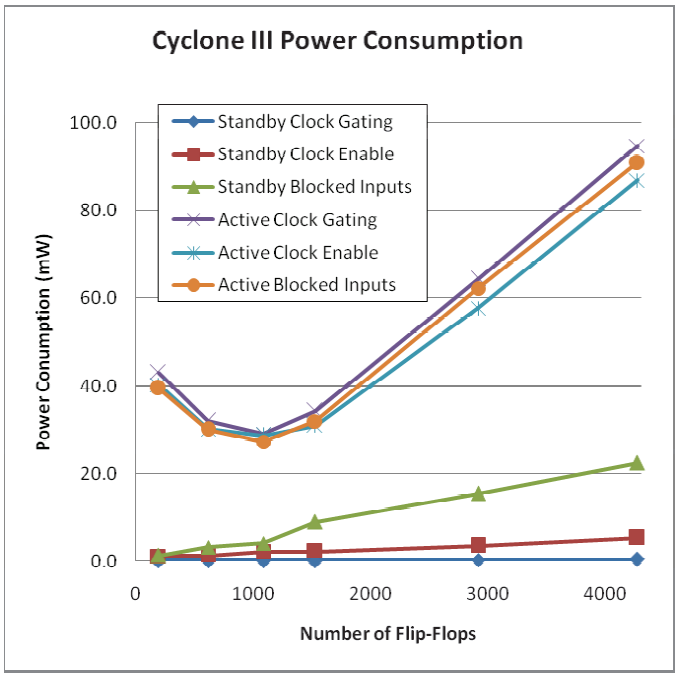

Figure 6. Cyclone III Standby and Active power consumption vs. Number of FF

An important implication of the study is that the use of pipelining, that adds a lot of flip-flops, reduces the power in active mode, but increases the power in standby mode. The balance between this is given by the amount of time in each mode.

The case of blocked inputs is different between Cyclone and Spartan. While in Spartan both cases are quite similar, in Cyclone CE is considerably better, but in all cases the power is proportional with the number of flip-flops.

ACKNOWLEDGMENT

The authors thank Gabriel Cutillas, from Silica, for his support on the Xilinx Spartan-6 LX16 Evaluation Kit.

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