Preliminary Studies on FPGA Implementation of a Real-Time Ultrasonic Air-Coupled Sonar

Krzysztof Herman, Eduardo Boemo, Washington Fernandez, Cristian Duran-Faundez, Ernesto Rubio

***Abstract*—This paper addresses some selected techniques for direction of arrival estimation using air-coupled ultrasound and custom hardware computational solutions. The main issue of the presented work is to perform a study of some hardware architectures capable to handle multichannel information processing in the real-time and its validation using experimental data.**

***Keywords*—air-coupled ultrasound, sonar systems, reconfigurable computing, FPGA, obstacle avoidance, digital signal processing,**

I. An introduction to air-coupled sonar systems

THE ultrasonic technology has been known for over 100 years and it is mainly oriented to underwater sonar systems, medical ultrasound and non destructive evaluation and testing, the air-coupled sonar systems are considered to be out of the ultrasonic mainstream technologies. This situation is mainly due to the ultrasonic waves characteristics [1] [2] and the properties of the gaseous medium [3]. Indeed, the principle problems related to the air-coupled ultrasounds are: (1) the high attenuation in the ultrasonic range of frequencies and (2) the impedance mismatch between gas medium and, in practice, any other kind of medium. However. gases tend to be linear over the wide range of acoustic pressure values, where only longitudinal waves can be propagated, what simplifies the analysis and solution of the wave equation.

Air-coupled sonar systems have a lot of inspirations in animal echolocation, especially, bats echolocation. Bats have developed an extraordinary echolocation performance being able to dynamically navigate in a three dimensional space and track a moving target incorporating various pursuit strategies [4], [5]. From the acoustics point-of-view the bats have two horizontally placed receivers and one central transmitter, what constitutes a highly reduced system to perform robust and accurate echolocation. Although the complete mechanism of bats echolocation is not completely understood (at the neurological level, for example), its general principles are well described. The main one is the ear shape, which determines directional characteristics of the receiver and, also, acts as an interferometer [6]. It is a known fact that most of the bats generate frequency modulated signals as echolocation pulses, what, together with a sophisticated neuronal mechanism, enables them to reach a range resolution of 0.2 mm and an angular resolution of 1.5 degrees and 3.5 degrees in horizontal and vertical directions, respectively [7]. More information about bats sonar signals and their applications in sonar systems can find found in [8].

Modern air-coupled sonar systems can be divided in two groups: (1) solutions based on a few receiving transducers followed by sophisticated signal processing algorithms to evaluate phase differences and hence, the angular information, and (2) solutions based on transducers arrays, where the angular information is being extracted using beamforming techniques. The first group of solutions represent the most classical way to implement air-coupled sonars, while the the second one (more complex) allows providing more information but requiring more sophisticated techniques.

The literature presents many examples of both cases. For the first one, in the paper [9] an echolocation system based on one transmitter and two receivers, incorporating frequency modulated signals was described. The presented solution was applied as a mobility aid for visually impaired people, where a digitized echo signal was down converted to the audible spectrum and presented to a subject (person) in order to perform localization experiments. One decade later, in [10] an interesting VLSI approach can be found to model bats auditory system in term of azimuth evaluation.

One of the first example of array based soultion was an implementation of air-coupled sonar system described in [11], where delay and sum beamforming method was applied to study echolocation performance. Other array based studies that incorporate beamforming can be found in the articles [12], [13], [14], [15], [16], [17]. In the paper [18] a linear array of MEMS microphone connected to a spatio-temporal filter was studied. The authors have realized signal processing using FPGA, however they focused mainly on array performance investigation and on proposing a low level, transistor based model for future studies. In the article [19] a comparison between two particular systems belonging to the two classes was made showing an equivalent performance echolocation, using information criterion as a measurement metric. Since the MIMO processing paradigm, due to its intrinsic parallelism can be considered to be processed using reconfigurable computing methods it is justified to incorporate these computational platforms in air-coupled sonars. The origin of this article has its origin in the lack of studies that performs the computational complexity and hardware cost of an air coupled ultrasonic systems dedicated for obstacle avoidance. In the context of this article it is worth to comment, that apart the article [18], the FPGA technology was incorporated in the following studies [20] and [21], however it was used only as a part of data acquisition module.

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II. Selected beamforming issues overview

Since the beamforming is one of the method of a sound source (an echolocation target) position estimation it will be short reviewed in this subsection. The most popular beamforming method is so called delay and sum beamforming given by eq. (2) [22]

$$B_k(n) = \sum_{m=0}^{M-1} w_m \cdot x_m(n - \tau_{m,k}). \tag{1}$$

The same equation can be represented in a graphic form Fig. (1) showing a difference between weighted and non-weighted version of data processing. To implement this method a

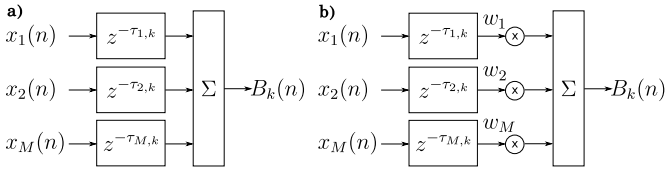

Fig. 1. Block diagram of delay and sum beamforming: a) without weighting, b) with weighting.

delay line has to be instantiated to hold the incoming signal samples history, what can be realized using various hardware design techniques. The multiplication is addressed only to the weighted version of the delay and sum beamforming, where delayed samples are being multiplied by fixed (or adaptive) weights $w_1 \dots w_M$. The weight application to each channel is a spatial version of windowing in order to perform the optimal trade off between side lobe width and grating lobes level of the spatial spectrum function. In the paper [23] a comparison of analogue and digital techniques for large arrays dedicated to process electromagnetic waves in RF band was presented. The authors of the above mentioned article have also performed a comparative study that favors digital beamforming processing methods in many aspects such as: implementation and calibration complexity, bandwidth, facilities for band pass correction. From the other side the analogue processing seems to be more energy and cost efficient. In the field of medical ultrasound systems, where large arrays of piezoelectric transducers are being incorporated, some current research [24], [25] underline the importance of the analog based beamforming techniques in high performance designs and propose new solution based on mixed signal technologies.

III. Reconfigurable computing methods

The reconfigurable computing methods allow to the programmer major flexibility in comparison with traditional methods of computation based on ISA (*Instruction Set Architecture*) exposed to the programmer. The programmable cores in the most cases imply sequentiality, what together with the finite instruction cycle generates long time periods. In the case of reconfigurable computing methods a reconfigurable fabric is being used to provide custom architecture development. The customized architecture can provide benefits like speedup (up to 500 times) and improved energy efficiency (up to 70 %) as it is reported in the paper [26]. The application performance improvements are possible thank to the problem parallelization (if possible) into separated threads, where each thread is being processed on a dedicated hardware. One of the example of problem parallelization is software loop unrolling, where instead processing the data in a closed N-length loop, N independent data paths are created together with a state machine, which controls the data flow. Not all problems can be parallelized due to its nature and ie. data dependency, what was the origin of System on Chip SoC fabrics, where an embedded processor(s), called programmable system (PS) and programmable logic (PL) share the same fabric. In such solution the parallelized parts of the problem are being offloaded from the PS and calculated on PL, while the rest of the algorithm is executed on (PS). The intercommunication between the PL and PS is established on Advanced eXtensible interface AXI, which is a part of Advanced Micro-controller Bus Architecture featured by ARM [27].

IV. Delay And Sum beamforming implementation on FPGA

This chapter describes implementation of some beamforming methods utilizing reconfigurable computing. The implementation was validated using real data captured by 32 ultrasonic sensor constituting linear array. All the details related to the input data capture methods are described in details in the article [14], where an off line analysis was performed to process the experimental data. Nevertheless some fundamental parameters of the experiment are essential to be recalled in this study. The goal of the experiment was to study horizontal DOA *(Direction of Arrival)* estimation performance. The linear array of 32 sensors was moved horizontally in front of a signal source capturing the sound pulses emitted by the source. The source signals were captured by the uniformly separated microphones followed by signal conditioners and AD converters using a sample rate of $f_s = 250\ kHz$ and 12 bit resolution. The sensors separation d was determined by sensor geometry and equal to $3.7\ mm$ The geometry of the experimental setup implies the change of the horizontal angle in a range of $< 0 - 14.5^\circ >$ withe a 0.32° resolution.

The Delay And Sum algorithm is the basic method of beamforming described by the eq. (1) where $B_k(n)$ stands for n-th sample of k-th beam that corresponds to a particular angle. The parameter M indicates number of sensors, $x_m(n)$ referes to n-th input sample of m-th microphone, $\tau_{m,k}$ describes a delay that corresponds to a particular angle at m-th sensor. The equation (1) can be expanded in to a sum of delayed samples as it is shown on eq. (2)

$$\begin{aligned} B_1(n) &= x_1(n - \tau_{0,1}) + ... + x_{M-1}(n - \tau_{M-1,1}) \\ B_2(n) &= x_1(n - \tau_{0,2}) + ... + x_{M-1}(n - \tau_{M-1,2}) \\ &\dots \\ B_K(n) &= x_1(n - \tau_{0,K}) + ... + x_{M-1}(n - \tau_{M-1,K}) \end{aligned} \tag{2}$$

At the hardware level the sum expansion can be considered as a fixed memory unit or a tapped delay line. Since the input signal is a uniformly sampled time vector it is necessary to explain the method for estimation of the variable delay $\tau_{m,k}$. The mentioned parameter represents angle dependent delay of the incoming wave front. For an uniformly spaced, planar

linear array the value can be estimated as it is shown on eq. (3)

$$\tau_{m,k} = \left[\frac{f_s d}{c} sin(\phi_k)^T \cdot m \right], \quad (3)$$

where c stands for sound velocity, ϕ_k is a column vector of all angles to be scanned (typically k is an odd number since angular scan is being done preserving symmetry), m is a row vector $< 0 - M - 1 >$ related to a subsequent sensor position and $[\cdot]$ symbol represents rounding to the nearest integer. Assuming that $\phi \in < -\phi_{(k-1)/2} \div \phi_{(k-1)/2} >$ the matrix of delays can be calculated on the fly or pre-calculated and represented in a form of a ROM look-up table. Since the sin function is an odd one the delay matrix represents odd symmetry as well, what can be utilized as a memory optimization method. A block diagram of a memory based

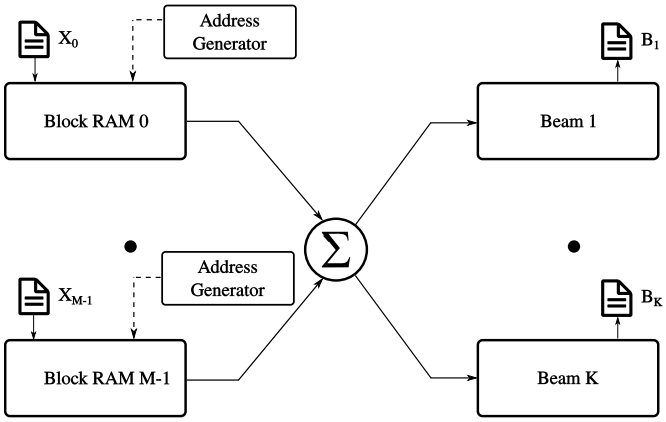

Fig. 2. Block diagram of time delay beamforming method implemented using block RAM and address generator.

architecture is shown on the figure (2), where Block RAM was utilized to hold the signals snapshot. The architecture was created utilizing Xilinx ISE 14.7 and tested in simulation mode using Xilinx ISIM tool. The main block of the presented design is the address generators, which generate an address that is send to each BRAM block to get the current or delayed sample.

V. Study Results

The simulation results obtained are divided into two parts: hardware specification and implemented functionalities.

A. Hardware specification

The clock analysis for the synthesized implementation shows the minimum period for the clock signal of 8.532 ns what corresponds to maximum operating frequency of 117.212 MHz. Selected macro statistics are presented in the table (I)

B. Validation of the system functionalities

The functionalities of the are presented on the following figures. The figure (3) shows the timing analysis of the beamforming module. The clk signal is set to 100 MHz and the input data fetching signal, which corresponds to the ce line, is being paced at 250 kHz. The beamforming delay and

TABLE I
Hardware statistics for the implementation developed.

Hardware component	Qty.
1024x16-bit single-port block Read Only RAM	32
2048x6-bit single-port distributed Read Only RAM	23
11-bit adder	23
11-bit sub-tractor	32
16-bit / 8-inputs adder tree	4
18-bit / 4-inputs adder tree	1
11-bit up counter	1
6-bit up counter	1
9-bit up counter	1
Flip-Flops	199
8-bit 2-to-1 multiplexer	5

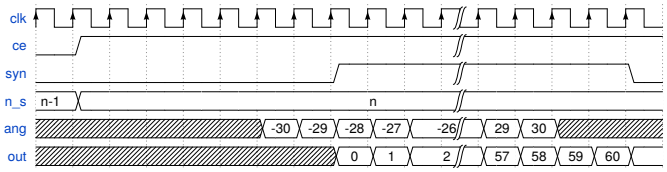

Fig. 3. Timing diagram of the beamformer block.

sum algorithm is being being processed at the sample rate for all angles from the range $-30°$ to $30°$ with a $1°$ step. The beamformer output is synchronized with sync signal, which can be interpreted as a data valid signal. Since the beamforming block calculates the sums at the clock rate the sync signal is active for 610 ns, what corresponds to 61 operations and is being coherent with the number of angular positions. Finally the sums for values for each sample and each steering angle is presented on the figure (4)

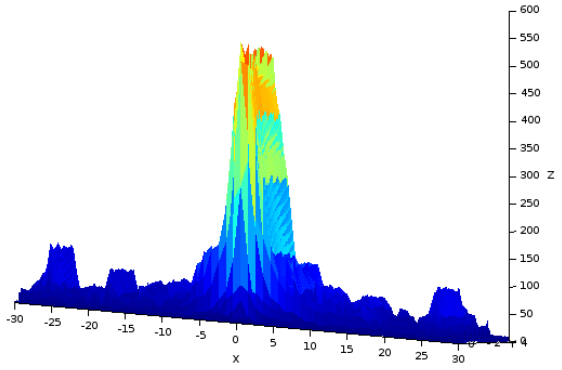

Fig. 4. The beamformer output for real signals calculated using the IP module developed.

VI. Conclusion

The presented study shows some partial results of the implementation of a beamformer applied in to real time air coupled sonar. Due to the low sound wave velocity the system frequency can be lowered decreasing the dynamic power consumption. Moreover the developed IP core is characterized

by a small hardware footprint and can be easily modified to be interfaced to an analog to digital converters. In this manner the presented method can be developed on programmable logic PL and controlled by programmable system PS thus instantiating a real time sonar for i.e a robotic platform. The further work encompasses development of more advanced beamforming methods and the study on the power characteristics of the IP cores developed.

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REFERENCES

[1] T. Gudra and K. Opielinski, "The range equation of the ultrasonic link in gas media," *Ultrasonics*, vol. 44, pp. e1423–e1428, 2006.

[2] T. Gudra, "Ultrasounds in gas media: generation, transmission, applications," *Archives of Acoustics*, vol. 33, no. 4, pp. 581–592, 2008.

[3] H. Bass, L. Sutherland, and A. Zuckerwar, "Atmospheric absorption of sound: Update," *The Journal of the Acoustical Society of America*, vol. 88, no. 4, pp. 2019–2021, 1990.

[4] J. A. Simmons, "The resolution of target range by echolocating bats," *The Journal of the Acoustical Society of America*, vol. 54, no. 1, pp. 157–173, 1973.

[5] J. A. Simmons and J. A. Vernon, "Echolocation: discrimination of targets by the bat, eptesicus fuscus," *Journal of Experimental Zoology Part A: Ecological Genetics and Physiology*, vol. 176, no. 3, pp. 315–328, 1971.

[6] G. Neuweiler, *The biology of bats*. Oxford University Press on Demand, 2000.

[7] J. Altringham, *Bats. Biology and Behaviour*. Oxford University Press Inc., 1999.

[8] G. Tadeusz, F. Joanna, and K. Herman, *Sonar systems*. InTech, 2011, ch. Bats Sonar Calls and its Application in Sonar Systems.

[9] T. Ifukube, T. Sasaki, and C. Peng, "A blind mobility aid modeled after echolocation of bats," *IEEE Transactions on biomedical engineering*, vol. 38, no. 5, pp. 461–465, 1991.

[10] T. Horiuchi and K. M. Hynna, "A vlsi-based model of azimuthal echolocation in the big brown bat," *Autonomous Robots*, vol. 11, no. 3, pp. 241–247, 2001.

[11] P. Webb and C. Wykes, "High-resolution beam forming for ultrasonic arrays," *IEEE Transactions on Robotics and Automation*, vol. 12, no. 1, pp. 138–146, 1996.

[12] M. R. Strakowski, B. B. Kosmowski, R. Kowalik, and P. Wierzba, "An ultrasonic obstacle detector based on phase beamforming principles," *IEEE Sensors Journal*, vol. 6, no. 1, pp. 179–186, 2006.

[13] K. Herman and L. Stach, "Analysis and elaboration of an air-coupled ultrasound wideband sensor array," *Acta Physica Polonica A*, 2011.

[14] K. Herman, T. Gudra, and J. Furmankiewicz, "Digital signal processing approach in air coupled ultrasound time domain beamforming," *Archives of Acoustics*, vol. 39, no. 1, pp. 37–50, 2014.

[15] J. Steckel and H. Peremans, "Ultrasound-based air leak detection using a random microphone array and sparse representations," in *SENSORS, 2014 IEEE*. IEEE, 2014, pp. 1026–1029.

[16] A. Unger, E. Konetzke, M. Rutsch, M. Hoffmann, S. N. Ramadas, S. Dixon, and M. Kupnik, "Versatile air-coupled phased array transducer for sensor applications," in *SENSORS, 2015 IEEE*. IEEE, 2015, pp. 1–4.

[17] J. Steckel, "Sonar system combining an emitter array with a sparse receiver array for air-coupled applications," *IEEE Sensors Journal*, vol. 15, no. 6, pp. 3446–3452, 2015.

[18] M. A. Clapp and R. Etienne-Cummings, "Single ping-multiple measurements: Sonar bearing angle estimation using spatiotemporal frequency filters," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 53, no. 4, pp. 769–783, 2006.

[19] J. Steckel, F. Schillebeeckx, and H. Peremans, "Biomimetic sonar, outer ears versus arrays," in *Sensors, 2011 IEEE*. IEEE, 2011, pp. 821–824.

[20] J. Steckel and H. Peremans, "A novel biomimetic sonarhead using beamforming technology to mimic bat echolocation," *IEEE transactions on ultrasonics, ferroelectrics, and frequency control*, vol. 59, no. 7, 2012.

[21] J. Steckel, A. Boen, and H. Peremans, "Broadband 3-d sonar system using a sparse array for indoor navigation," *IEEE Transactions on Robotics*, vol. 29, no. 1, pp. 161–171, 2013.

[22] D. H. Johnson and D. E. Dudgeon, *Array signal processing: concepts and techniques*. PTR Prentice Hall Englewood Cliffs, 1993.

[23] K. Zarb-Adami, A. Faulkner, G. Kant, P. Picard *et al.*, "Beamforming techniques for large-n aperture arrays," in *Phased Array Systems and Technology (ARRAY), 2010 IEEE International Symposium on*. IEEE, 2010, pp. 883–890.

[24] J.-Y. Um, Y.-J. Kim, S.-E. Cho, M.-K. Chae, B. Kim, J.-Y. Sim, and H.-J. Park, "A single-chip 32-channel analog beamformer with 4-ns delay resolution and 768-ns maximum delay range for ultrasound medical imaging with a linear array transducer," *IEEE transactions on biomedical circuits and systems*, vol. 9, no. 1, pp. 138–151, 2015.

[25] Z. Yu, M. A. Pertijs, and G. C. Meijer, "A programmable analog delay line for micro-beamforming in a transesophageal ultrasound probe," in *Solid-State and Integrated Circuit Technology (ICSICT), 2010 10th IEEE International Conference on*. IEEE, 2010, pp. 299–301.

[26] T. J. Todman, G. A. Constantinides, S. J. Wilton, O. Mencer, W. Luk, and P. Y. Cheung, "Reconfigurable computing: architectures and design methods," *IEE Proceedings-Computers and Digital Techniques*, vol. 152, no. 2, pp. 193–207, 2005.

[27] Xilinx, *Zynq-7000 All Programmable SoC Technical Reference Manual*.