Editorial

Field-programmable logic and applications

Since their inception in the 1980s, field programmable gate arrays (FPGAs) have emerged to be a mainstream technology for implementing digital systems. Commercial demands together with Moore's Law have led to great improvements in their capacity and functionality. Research in the areas of architecture, CAD tools, compilation, design techniques and applications is vitally important to address issues associated with technology scaling, designer productivity and to push the boundaries for innovative uses and performance.

This Special Section contains five papers that constitute advances in field programmable logic systems, taken from the 16th International Conference on Field Programmable Logic and Applications (FPL) which was held 28–30 August, 2006 in Madrid, Spain. The papers cover important contemporary problems including process variations, floorplanning, dynamic reconfiguration, hardware compilation and random number generation.

A major issue associated with VLSI technology scaling is that the variation in transistor characteristics increases as feature sizes are reduced. The first paper by Lin *et al.*, applies statistical timing analysis to create an analytic timing yield model which is then used for variation aware placement. They show that this new placement scheme, which advantageously uses the reprogrammable nature of the FPGA, can achieve a yield loss which is 29.7% of the original for guard-banding and 4% of the original with speed-binning.

One feature of field programmable gate arrays (FPGAs) is their potential for dynamic reconfiguration; that is, reprogramming part of the device at run-time so that resources can be reused through time multiplexing. The second paper by Singhal and Bozogzadeh, describes a framework for floorplanning dynamically reconfigurable designs. They introduce a multi-layer sequence pair representation for considering multiple designs simultaneously and apply simulated annealing to minimise the number of reconfiguration bits required, while considering other factors such as area and wire length.

The third paper, by Danne *et al.*, is also concerned with dynamic reconfiguration. It presents a scheduling technique for the execution of periodic real-time tasks with dynamic reconfiguration. The run-time system, implemented in hardware, is able to perform preemptive multitasking. Reconfiguration overheads, such as device reconfiguration and context switching are considered. A practical implementation that processes and displays frames of videa data is described.

In the fourth paper, Baradaran and Diniz present a hardware compilation scheme that combines high-level compiler techniques with low-level scheduling information. The scheme applies a set of data-oriented transformations guided by the critical path of the computation. Transformations are applied to efficiently map data to registers, internal RAM and off-chip RAM while minimising execution time and considering available storage and bandwidth.

The final paper, by Thomas and Luk, addresses the application level issue of generating non-uniform random numbers. Using piecewise linear approximation, the scheme allows random number generators with arbitrary distributions to be constructed. Furthermore, the resulting generators are compact, high speed and the distribution can be rapidly changed at run-time.

These papers are a subset of the many interesting papers presented at the FPL conference. We hope that you will find them interesting. We would also like to take this opportunity to thank the authors and reviewers as well as the editorial staff at the IET for their help in compiling this special section.

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Andreas Koch received his diploma in informatics and his doctorate from the Technical University of Braunschweig (Germany) in 1992 and 1997, respectively. He then joined the CS department of UC Berkeley as a post-doctoral researcher, participating in architecture and tools research for adaptive computers. In 1999, he returned to Braunschweig for his habilitation, which he attained in 2005. That same year, he joined the Technical University of Darmstadt (Germany) as a professor, founding the Embedded Systems and Applications research group. He continues his work on reconfigurable computing in the areas of systems architecture, high-level and physical design tools, and application evaluation. Dr Koch was program co-chair for the 2006 International Conference on Field-Programmable Logic and Applications and co-chaired in 2007 the 4th Workshop on Dynamically Reconfigurable Systems. He has served in program committees for conferences such as DATE, DAC, RAW, SAMOS, and FPL, and acted as reviewer for both IEEE and ACM publications.

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