Thermal Monitoring on FPGAs Using Ring-Oscillators

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Abstract. In this paper, a temperature-to-frequency transducer suitable for thermal monitoring on FPGAs is presented. The dependence between delay and temperature is used to produce a frequency drift on a ring-oscillator. Different sensors have been constructed and characterized using XC4000 and XC3000 chips, obtaining typical sensibilities of 50 kHz per °C. In addition, the utility of the Xilinx OSC4 cell as thermal transducer has been demonstrated. Although a complete temperature verification system requires a control unit with a frequency counter, the use of ring-oscillators presents several advantages: minimum FPGA elements are required; no analog parts exists; the additional hardware needed (multiplexers, prescaler, etc.) can be constructed using the resources of an FPGA, the thermal-related signals can be routed employing the standard interconnection network of the board, and finally, the sensors can be dynamically inserted or eliminated.

1 Introduction

Lower operating temperature on CMOS devices reduces the intrinsic delay and interconnection resistance. It also produces important reliability improvements, considering that electromigration and other failure effects rise exponentially with the temperature [1]. In the area of FPGAs, the gate density and speed of recent devices have appended thermal considerations to the traditional design trade-offs. Applications that make intensive use of chip resources at high speed can dissipate beyond current packaging limits. Miniature heat sinks and fans originally developed for the high-end microprocessor market are becoming familiar in the area of fast-prototyping.

The thermal considerations presented above results enlarged on FPGA-based systems like custom computers (FCCMs) and logic emulators. Their exhaustive utilization of dynamic reconfiguration increases the risk of configuration errors and signal contention. These situations may cause a significant increment of temperature and can produce a permanent chip damage. Moreover, like occurs on a single FPGA, the consumption associated to a given machine configuration is a priori unknown; thus, the particular features of an implementation (fine-grain pipelined datapaths, heavily loaded buses, etc.) can produce an unforeseen power overhead. Consequently,

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the implementation of a thermal monitoring unit allows several failures in FCCMs to be detected. For example, this strategy has been adopted in the XMOD board [2]: an 8-bit CPU examine the both the temperature and current at each FPGA.

Considering that the processing tasks on a multiple-FPGA board are performed in several chips, the detection of hot-spots requires to sense the temperature in each FPGA that composes the system. However, if the number of chips is relatively high, it is difficult to use discrete thermal transducers, as is common on current PC boards. Thermocouples or integrated sensors require both extra wiring and hardware that must be immune to the influence of the high-frequency signals usually present on the board. Moreover, the designer must also pay attention to topics beyond the scope of the fast-prototyping area, like sensor positioning, thermal coupling, or analog instrumentation.

The implementation of on-chip thermal transducers allows the designer to avoid the inconveniences described above. Main techniques to construct temperature sensors on CMOS technology make use of analog effects like the temperature dependence of the junction forward voltage, or the Seebeck effect [3]. Although these ideas can be useful to FPGA architects, they appear inadequate to the end-users of commercial chips. In this paper, this limitation is overcome by using ring oscillators as temperature transducers. This type of circuits can be easily implemented using few FPGA elements. The advantages of this approach are multiple:

a. Like other on-chip sensors, the junction temperature instead of the package one is measured.
b. All signals are digital; thus, they can be routed using the general interconnection network of the board.
c. The sensor itself is small: practical circuits make use of one or two logic blocks, and a minimum-size sensor can be fitted in just an I/O block.
d. The hardware needed to centralize the thermal status of the machine (basically a multiplexer and a prescaler counter to reduce the frequency) can be mapped in the FPGA, meanwhile the remaining low-speed tasks can be performed by the host or using a low-cost microcontroller.
e. A sensor or even an array of them can be placed in virtually in any position of the chip, making possible to construct a thermal map of the die.
f. The sensor can be dynamically inserted or eliminated.

Several researchers have proposed the use of on-chip thermal transducers. In [4], ring oscillators are used to measure both the temperature and power supply fluctuations. The oscillator is activated during a fixed period, and a counter with an scan path is used to read back the resulting frequency. In [5], an approach based on a “thermal-feedback oscillator” have been developed, whose main advantage is the small dependence between frequency and power supply fluctuations. At PCB level, a thermal monitoring method based on the measurement of a copper trace resistance has been proposed in [6]. In a different context, the use of thermal testing to detect gate oxide short failures have been proposed in [7].

Table 1. Ring-oscillators constructive characteristics

Test Circuit	Chain of inverters	Wiring
s1 and s5	Three inverters. Mapped in two CLBs.	General interconnection. Long delays.
s2 and s6	Three inverters. Mapped in two CLBs.	General interconnection. Short delays.
s3	Three inverters. Mapped in two CLBs.	Three long-lines plus one direct-line.
s4 and s7	One inverter. Mapped in a IOB output buffer.	General interconnection. Short delays.
OSC4	Internal cell.	General interconnection.

Table 2. Ring-oscillators features

Test Circuit	Experiment goals
s1 and s5	Medium-size, low-frequency sensor.
s2 and s6	Compact-size, medium-frequency sensor.
s3	Long-line based sensor. Suitable for clocking a synchronous counters without using the dedicated clock lines.
s4 and s7	Minimum-size. Worst-case sensor (maximum allowable frequency).
OSC4	XC4000 internal 5-frequency clock-signal generator cell

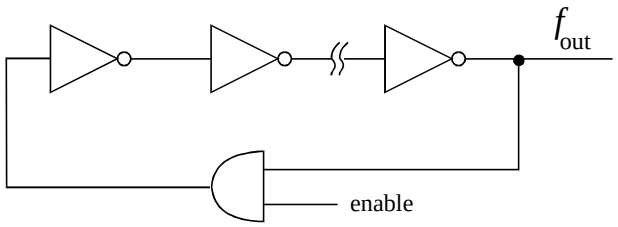
Table 3. Ring-oscillators timing characteristics

Test Circuit	Net delays (*Xdelay* tool)	Combinatorial delays (*Xdelay* tool)	Chip sample
s1	50.7 ns	22 ns (four LUTs)	XC3030PC84-125
s2	14.4 ns	22 ns (four LUTs)	XC3030PC84-125
s3	17.9 ns	22 ns (four LUTs)	XC3030PC84-125
s4	12 ns	8 ns (one obuf + one ibuf)	XC3030PC84-125
s5	47.8 ns	24 ns (four LUTs)	XC4005PC84-6
s6	20.1 ns	24 ns (four LUTs)	XC4005PC84-6
s7	10.8 ns	9 ns (one obuf + one ibuf)	XC4005PC84-6

2 Ring-oscillators on FPGAs

A ring-oscillator basically consists on a feedback loop that includes an odd number of inverters (Fig.1). Thus, the necessary phase shifting to start the oscillation is produced. The oscillation period is twice the sum of the delays of all elements that compose the loop.

Fig. 1. A ring-oscillator scheme



Ring-oscillators can be mapped on FPGAs using the look-up tables or the programmable inverters included on the I/O blocks. Considering that different interconnection elements can be inserted in the loop, the number of possible implementations are extremely large. In order to restrict the experiments, in this work just four different circuits, called s1, s2, s3 and s4, were characterized in the XC3000 family, and three circuits versions (s5, s6 and s7) where selected for the XC4000 family. In addition, the thermal response of the 8-MHz output of the built-in clock signal generator OSC4 [8] was measured. Main circuit features are summarized in Tables 1, 2 and 3.

An external control signal was *ANDed* with the loop in all CLB-based test circuits s1, s2, s3, s5 and s6, in order to allow the oscillators to be stopped. As a consequence, although these circuits have three inverters, their loops include four LUT delays. In the IOB-based oscillators s4 and s7, the loop was opened by using the 3-state control of the output buffer. These IOB versions were constructed to analyze the performance of the minimum allowable sensor size. All circuits were placed in the chip border in order to minimize the wiring capacitance between the oscillators and the corresponding output pads. As example, the layouts of the XC4000 oscillators s5, s6, s7 and osc4 are depicted in Fig.7

3 Experimental Results

The frequency-to-temperature response of each sensor was obtained by introducing each FPGA in a temperature-controlled oven. An Iron-Copper/Nickel (*Iron-Constantan*) thermocouple probe was placed in the center of the package, and

was fixed to it with a heat conductive silver epoxy. An study about mechanical details of thermal sensors can be found in [9].

Fig. 2. Output frecuency vs. Temperature.
XC3090-125 CLB-based oscillators s1, s2 and s3

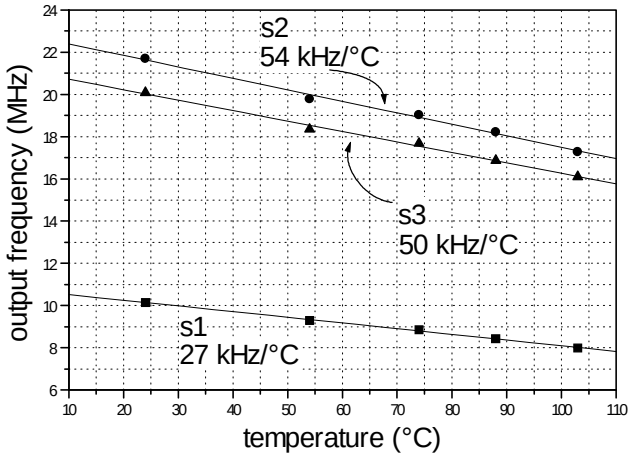


Fig. 3. Output frecuency vs. Temperature. XC4005-6
CLB-based oscillators s5, s6 and OSC4 cell

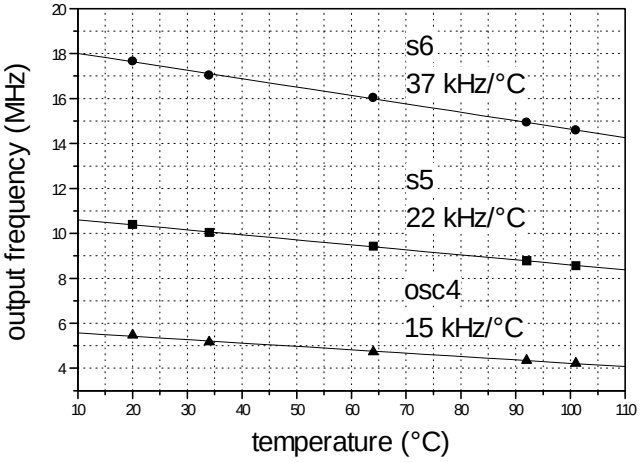
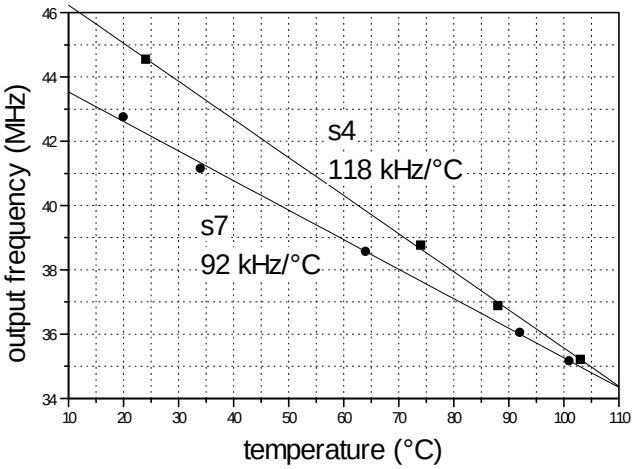


Fig. 4. Output frecuency vs. Temperature. XC4005-6 and XC3090-125 IOB-based oscillators s4 and s7



A long ribbon cables (near 0.8 meters) were utilized to carry both output and control signals outside the oven. In order to prevent an excessive sensor power consumption due to these high off-chip loads, a driver 74HC125 was inserted to isolate the FPGA from the cables.

Each FPGA was configured with all oscillators versions, but just one was enabled during the short period of time necessary to accomplish the frequency measurement. After that, the corresponding circuit was stopped again in order to maintain uniform the chip temperature. It allowed the error produced by self-heating to be minimized. An x-t curve tracer was utilized to verify the thermal equilibrium in the system after each temperature step. The error in the temperature measurement was maintained near 1 °C.

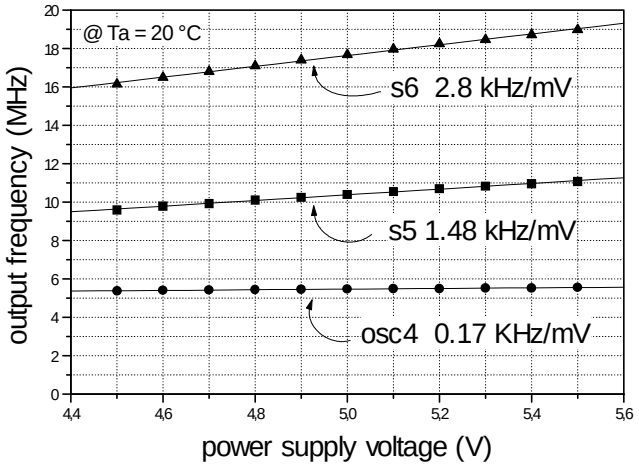
In Figs. 2, 3 and 4, the main experimental results are shown. All sensors exhibit a quite linear dependence with the temperature in the normal range of operation. The temperature sensitivity (in percentage per °C) also is very similar for all circuits. However, the IOB-based circuits, s4 and s7, present a high frequency oscillation, over 40 MHz, and should be discarded for practical applications.

The CLB-based sensors have relatively high speed (between 10 and 20 MHz), although their frequencies can be easily managed by a low-cost microcontroller if a prescaler is used. For example, a popular 68HC11 can be employed for counting if all these frequencies are previously divided by ten.

The best results corresponded to the built-in OSC4 cell. This oscillator, not only runs at lower speed and do not make use of extra FPGA resources, but also exhibits a small sensitivity to power supply fluctuations. The use of this cell as thermal transducer have not be reported in the manufacturer data books.

The power supply dependence of all sensors resulted linear in the operation range. This is depicted in Fig.5 for the XC 4005-6 oscillators. Thus, errors caused by power supply fluctuations can be corrected if the voltage of the board also is monitored. However, the sensibility was smaller for the OSC4 cell, as is depicted in Table 4. In addition, was observed that sensors whose loop delay is mainly caused by wiring are slightly less susceptible to power supply fluctuations.

Fig. 5. Output frecuency vs. power supply voltage.
XC4005-6 oscillators s5, s6 and OSC4 cell.

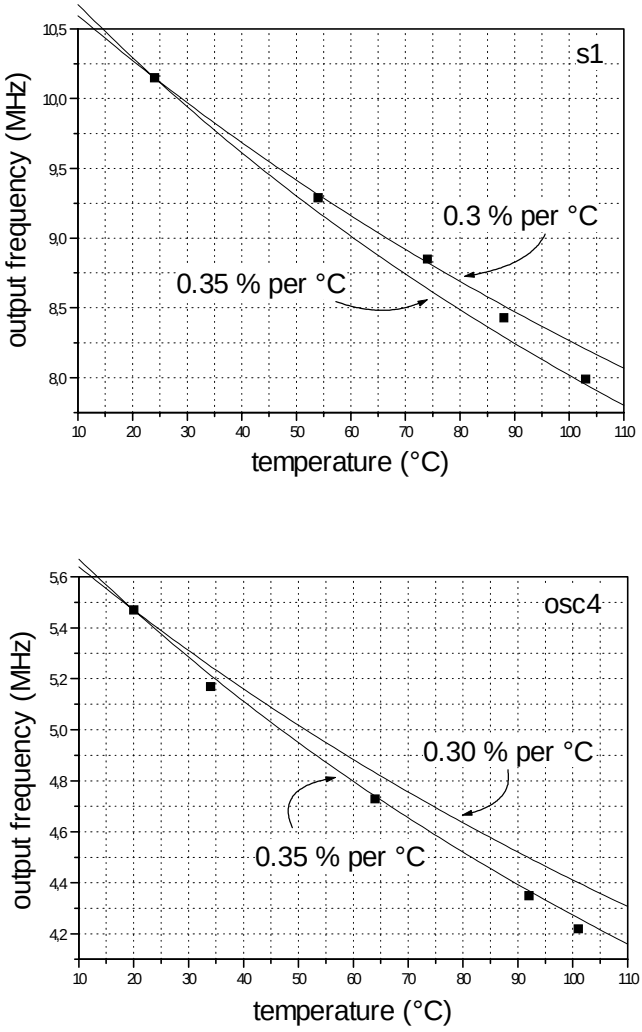


An alternative method for the temperature calibration of a given sensor can be carried-out if the approximate CMOS delay coefficient given by the manufacturer is utilized. This value is situated between 0.3 % per °C [10], and 0.35 % per °C [11]. In this way, the designer must first to construct a particular oscillator, and then to measure its output frequency at a known room temperature. After that, the remaining pairs (T,f) can be calculated by applying the delay coefficient to the measured point. Two examples of this method are shown in Fig.6.

Table 4: Output frequency reduction at Vcc=4.5 V

Test circuit	Frequency reduction at Vcc=4.5V in relation to normal operation
osc4	-1.8 %
s1	-7.3 %
s5	-7.8 %
s2	-7.9 %
s3	-8.1 %
s6	-8.7 %

Fig. 6. Measured (square points) and predicted oscillation frequencies (lines) vs. temperature using the CMOS delay coefficient. Circuits s1 and OSC4. Output frequency at room temperature as reference point.



4 Conclusions

A group of experiments to demonstrate the feasibility of on-chip temperature transducers based on ring-oscillators have been presented. The proposed circuits allow the junction temperature of an FPGA to be easily measured. All prototypes analyzed showed a linear response with the temperature.

Although two methods for sensor calibration have been described, they can be simplified if the goal is just to detect a peak power value. In that case, the adjustment can be done in terms of power consumption, by measuring both chip input current and sensor output frequency during the normal operation of a given application. Thus, the

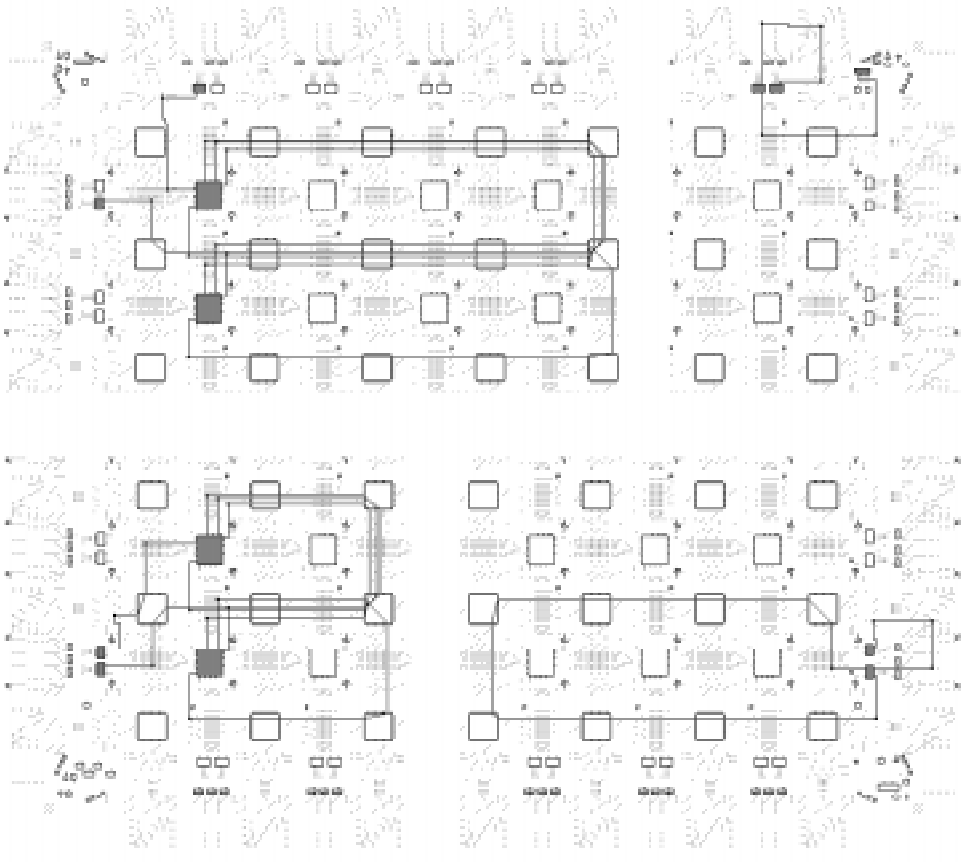
correct thermal status of the machine can be described by a range of expected frequency values in each FPGA.

Best results in frequency range, resource occupation, and power supply sensitivity corresponded to the built-in XC4000 oscillator. However, the main disadvantage of this circuit is their fixed position in a corner of the chip. On the contrary, CLB-based ring oscillators can be situated in virtually any position.

The combination of temperature transducers and FPGAs could be also a powerful tool for researchers interested in thermal aspects of integrated circuits and packaging. Just the possibility of "moving" a sensor (or an array of them) from one point of the die to other, in a simple, fast and inexpensive way, is almost unthinkable in any other VLSI technology.

Future work will include a comparative study of die thermal maps using ring-oscillator sensors and an IR microscope.

Fig. 7. Layout of the s5 (top. left), s6 (bottom, left), s7 (bottom, right) and osc4 (top, right) oscillators (shaded areas represent used resources of the FPGA)



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