Learning VLSI Design Using Programmable Logic Arrays

Eduardo I. Boemo Juan M. Meneses
E.T.S.I. Telecomunicación

1. INTRODUCTION

This paper describes technical aspects, organization details and results of an experimental undergraduate laboratory based on Field Programmable Gate Arrays (FPGAs), at the School of Telecommunication of Madrid, Spain. The target of the course has been to introduce concepts of ASIC design methodology like hierarchy, modularity, simulation and testability, using a low alternative and a design-oriented, hands-on learning approach.

Many universities offer VLSI courses based on Mask Programmed Gate Arrays (MPGAs) or Standard Cells. They usually have a strong relationship with foundries and CAD Tool manufacturers [1]-[2] or are integrated on educational actions like the MMC [3] or Eurochip [4] in Europe (A complete set of european VLSI teaching surveys can be found in [5]). Nevertheless, managing a VLSI laboratory is a complicated and expensive task. Professional CAD tools, test instruments and prototype prices are high even though reduced educational prices exist. VLSI laboratories imply an organizational overhead and require intensive professor dedication as well as high professor/student rates, due to the inherent complexity of the subject. Consequently, it is not easy to create a laboratory to deal with a great quantity of students.

The appearance in the market of high density FPGAs like the XC4000 [6] or the FLEX 8000 [7] marks a new age of electronic teaching. Although they were developed for the industrial market, they have became an ideal solution for education laboratories. Main advantages of FPGAs over MPGAs are: their CAD tools can run on Pcs; they can be configured without the participation of silicon foundries; it is possible to recycle the prototypes; and their fast design cycle allows efficient use of the laboratory time.

FPGAs allow every educational institution to offer a low-cost, ASIC-like design course, not only for future specialists but also for all students in Electrical Engineering and Computer Science, thus providing a generalist education for future engineers. Finally, the use of FPGAs is a realistic teaching approach for universities of developing countries where electronic industries are incipient, there is no access to silicon foundries and the local market size does not justify the use of other ASIC solutions.

2. FPGAs: A BRIDGE TO THE VLSI WORLD

Principal consequences of VLSI advances, from the point of view of electronic system designers, have been complexity growth and the difficulty to close the classical loop design-implementation-verification. It has been imperative to move the electronic design from art toward a fixed methodology. This evolution has stated new challenges in engineering education. In order to determine if a FPGA laboratory can contribute to the learning of VLSI design themes, it is necessary to evaluate the following points:

Design Flow: FPGA software follows a design flow very similar to any other ASIC development tool. It permits exercising all typical stages of VLSI design and their interactions: specification, design entry, logical simulation, place and route, post-layout simulation, implementation, testing and generation of complete documentation.

Methodology for handling complexity: Although the density of FPGAs is still poor compared with MPGAs (where the integration level can be 10 times higher), the increasing density of FPGAs, now over 20,000 "equivalent" gates, makes it possible to manage circuits with a suitable level of complexity. All the suggestions indicated in the well-known Mead and Conway design approach [8] are also valid in this technology. FPGAs evidence the advantages of hierarchical, partitioned, synchronous and regular solutions. Students can see the advantages of abstraction, the use of a divide-and-conquer strategy, the top-down decomposition and the avoidance of superfluous sophistication.

CAD Tools: FPGAs permits hands-on design with a powerful, modern professional tools. This training is vital; currently, all areas of engineering are supported by CAD tools, and the designer depends on these tools to surmount the increasing complexity of contemporaneous electronic systems. In education, it is very important to support the training in genuine (not perfect, not didactic and not well documented) professional design tools.

0-7803-1482-4/93/$3.00 © 1993 IEEE

Thus, the laboratory attempts to reproduce an ordinary situation in the actual engineering world: to solve an unknown problem with an unknown tool (with inevitable puzzling error messages, mysterious bugs and labyrinth manuals). The development of this skill is one of the most valuable goals of a laboratory. Students can experiment the increasing gap between the draft design and the actual implementation of complex systems.

Design for Testability (DFT): FPGAs are tested devices and no fault simulation is necessary. However, the main DFT columns: observability and controllability, are essentials on FPGA design. Students can learn some ad-hoc techniques in order to simplify circuit testing, like splitting counters, remembering the system reset signal, adding external control signals or checking incompatible combinations of signal values. Other techniques like Scan Path or BILBO [9] can be introduced by implementing case-study circuits on FPGAs. In summary, although testing is strongly coupled to high a density IC design, some of the themes about DFT teaching [10]-[11] can be sustained by a FPGA based laboratory.

Mixed Digital/Analog Design: This is still not possible with the product currently on the market. Consequently, the scope of the laboratory is limited to digital design.

Hardware Description Languages: The growth of system complexity forces the designers to use hardware description languages in order to clarify the system specification. In FPGAs, some HDL synthesis tools are available.

Training on CAD Algorithmic: FPGAs offers the students the possibility of designing or evaluating CAD tools and algorithms. They can create module generators for counters, adders, multipliers or other regular structures, and then integrate the resulting file in the standard design flow in order to route it. Furthermore, they can test the ability of the standard tools by implementing a circuit with different placement and routing strategies and comparing simulation results.

Tendency: Although the FPGA market is about 3% of the MPGA market size, nowadays one-half of the chip designs has begun using programmable logic devices [12]. Moreover, FPGAs are currently a gateway to MPGA because many foundries now are offering FPGA retargeting. Finally, programmable logic circuits have opened suggestive horizons where they are insurmountable: dynamic reconfiguration circuits and fast prototyping. Both applications by themselves justify the inclusion of programmable logic in an EE curriculum. Although there are some negative points, the balance is very positive. FPGAs cannot substitute a broadband VLSI course (analog design, full-custom, AsGa, BICMOS, DFT Techniques, etc.) but can replace or complement an MPGA course. Nowadays, the emergence of educational laboratories based on FPGAs is a worldwide tendency. An impressive example is [13].

3. ADJUSTING A PROFESSIONAL TOOL FOR EDUCATIONAL LABORATORIES

Our FPGA course is supported by Personal Computers. In order to maintaining the integrity of the PC software, a set of security routines has been developed [14]. It permits the setting of a permanent, read-only status to application programs and libraries; the implementation of an access control list for users, groups or superuser; the establishment of passwords; the confidentiality of user files; and complete virus immunity. The protection strategy is software based and just requires one simple change to the PC hardware in order for it be fully operative.

In order to protect the hardware part of the LCA design course, a training board based on the XC3020PC68-50 was developed. This chip [15] was selected because of its low cost and minimal requirements relative to the PC (principally memory and processing speed). The main characteristics of the board are: optocoupled I/O, PC bit-serial configuration capacity, and LEDs and 7-Segment displays for user applications. Another board for eprom-programming and daisy-chaining was also developed.

Both software and hardware protection schemes added reliability and allowed the adaptation of professional tools for use in an overcrowded educational laboratory. The last protection action was to hide the anti-copy keys, by putting it inside the PC and connecting it to the external port via a cable.

4. SCOPE OF THE COURSE

The topics covered in the classroom are listed in Table I. The complementary sessions in the laboratory are divided in two parts: First the students follow a tutored example [16] of a 16-bit counter whose structure, at the gate-level, must to be a copy of the well-known 74163. The goals are to force the designer to acquire experience with the Xilinx development tool and allow a comparison in size, cost, performance and design time with respect to the standard off-the-shelf TTL solution. In the second part, the students must solve and implement a proposed design; so they are face-to-face with a complex problem that usually has potential regularity and modularity. After finishing the work, students can probe the equivalent Altera development system.

The course is oriented to the design of a complete system instead of a collection of small examples. The successful resolution of such a problem which involves different trade-offs is a good exercise of analysis, knowledge, astuteness and intuition. It gives students the useful information and skill required to understand and estimate the complexity of future VLSI designs.

Introduction	Time-to-Market and Concurrent Engineering. The Sources of Errors on Electronic Design. Programmable Logic Circuits: Evolution and Revolution in R&D. Products and Companies. Impact on Design Methodology and Production.
Architecture	Switch CMOS. Look-up Tables. XC3000 Family: Internal structure: CLBs, IOBs and Interconnection Resources. Skew and Clock Lines. Configuration. XC4000 and Flex 8000 Families.
CAD Tool	Top-down and Bottom-up Design. Schematics vs. HDLs. Software Structure. Synthesis, Partitioning, Placement and Routing. CAD Algorithms. Xilinx File Organization. Module Generators. XACT.
Simulation	Prelayout and Postlayout Simulation. Design for Testability: Observability and Controllability. Ad Hoc Techniques. Additional Logic for Testing. Scan Path.
Design I	Hierarchy. Synchronous Design. FPGA-Structure Oriented Design. I/O Possibilities. Routing Directives. Including PALs. Configuration: Serial, Parallel and Daisy-chain.
Design II	Manual Placement. Pull-up, Wire-and and Buses. Map-then-merge and Merge-then-map. High Speed Design. Pad or Core Limited Circuits. Encapsulates and Electrical Characteristics.
Computer Arithmetic	Adders. Multipliers: Wallace, Booth, Dadda and Iteratives. Pipelining. Systolic Arrays. Skewing and Deskewing Registers. Latency and Throughput. Cost Functions. Bit-Serial Arithmetic. Self-timed Circuits.
Conclusions	XC3000 vs. XC4000. FPGAs vs. Standard Cells. APR vs. CLBMAP+AR. PREP Benchmarks. Independent Vendors Tools. Perspectives.

Table I: Undergraduate Course: "Introduction to FPGA Design"

5. SPECIFYING A FPGA LABORATORY

In order to design a new laboratory and calculate its cost, the following "mathematical model" can be used:

$$M = \frac{P\,T_2}{J\,S\,T_1\,T_3}$$

Where:

- M number of stations
- P number of students
- J number of turns per day.
- T_1 number of hours of each turn.
- S number of students per group.
- T_2 average time in hours required to finishing the training.
- T_3 Number of days assigned to the course.

In our case, the laboratory is open from 9 AM to 9 PM. The working day is divided in 4 turns of 3 hours each. Each turn is assigned to a group of two students. In order to measure the learning, a test course with 20 selected students was organized. The average time to complete the tutorial was about 15 hours. Assuming 50 hours to finish the training (tutorial plus the design case) we estimated the needed for equipments in 20 design stations. It permitted us to attend over 400 students per course (the laboratory is compulsory all students of the school), scheduling 44 days for FPGAs, and then to continue with the complementary part of our laboratory (design of a microprocessor controlled systems).

Based on the supposition that PCs and software can be utilized for 3 years, the cost/student of our training is about $ 30 (it does not take into account professor and assistant costs). This is an incredible price for an ASIC-like course. Note, on the other hand, that the amortization period is quite conservative; although fitting and routing algorithms are being improved every day, the concept involved in the design methodology will continue invariably. The use of non-updated software tools will not have serious educational consequences.

6. RESULTS AND CONCLUSION

The results of the FPGA course have been highly positive. The student's response has been very enthusiastic and they have spend a lot of time in the laboratory. They have designed and tested a great variety of interesting circuits. Some of the principal works presented were: Frequency Multipliers, Arithmetic Logic Units, Time-of-Day Clocks, Static RAMs, Fast Counters, Binary-Morse Converter, Pixel Averager, Pipelined Circuits, Systolic Adders and Multipliers (great variety), Microprocessors Parts, FIR Filters, Bit-Serial Arithmetic Circuits and several Module Generators for Adders, Counters, State Machines, Decoders and Shift Registers.

The first course started in 1990, and currently it is part of Year 3 of the EE Degree. The laboratory has also been successfully included in our continuing education program oriented to secondary school professors. The impact of FPGAs over the promotion of the VLSI education activities of our Department will be evaluated in a few years.

REFERENCES

[1] M. O'Keefe, J. Lindenlaub, S. Bass and T. Wahlen. "Introducing VLSI Computer-Aided Design into the EE Curriculum: A Case Study". *IEEE Trans. on Education.* pp.226-236. Vol. 32. Nº3. August 1989.

[2] A. Rucinski. "A Course in VLSI Semicustom Design in a Small School Environment". *IEEE Trans. on Education.* pp.93-100. Vol.31, n°2. May 1988.

[3] R. Chiang, D. Cunningham, B. MacDonald and K. Weiss. "A Partnership Approach to Engineering Education: Microelectronics Programs in Massachusetts". *Proc. Frontiers in Education Conference 1992.* pp.750-755. IEEE Press 1992.

[4] B. Courtois. "CAD and Testing of ICs and Systems. Where are we going?". *Report CMP*, pp.59-62. Grenoble, France. January 1993.

[5] "Teaching and Research Initiatives in VLSI Design". (Special Issue on Education). *IEE Proceeding.* Part G. Vol.139. Nº2. April 1992.

[6] *"The XC4000 Data Book"*. Xilinx Inc. 1992.

[7] *"Applications Seminar. Fall 1992"*. Altera Corporation. 1992.

[8] C. Mead and L. Conway. *"Introduction to VLSI System"*. Reading, MA. Addison-Wesley. 1980.

[9] T. Williams and K. Parker. "Design for Testability. A Survey". *IEEE Trans. on Computer.* Vol.C-31, No.1, pp.2-15. January 1982.

[10] Serra M. "VLSI Design and Test: A Unified Approach". *IEEE Trans. on Education.* Vol.32, No.3, pp.237-245. August 1989.

[11] R. Absher. "Test Engineering Education Is Rational, Feasible, and Relevant". *IEEE Design & Test of Computers,* pp.52-62. December 1991.

[12] S. Brown, R. Francis, J. Rose and Z. Vranesic. "Field Programmable Gate Arrays". *Kluwer Academic Publishers,* Norwell, Massachusetts, 1992.

[13] D. Van den Bout, T. Nagle, T. Miller and P. Franzon. "The NCSU Design Centre". *Int. Report. Dept. of Electrical and Computer Engineering.* North Carolina State University. 1992.

[14] E. Boemo, F. Barbero and J. Meneses. "Software Security Strategies for PC-Based Educational Laboratories. A Case Study". *Proc. Frontiers in Education Conference 1993* (this issue). IEEE Press 1993.

[15] *"The Programmable Gate Array Data Book"*. Xilinx Inc. 1992.

[16] E. Boemo, F. Barbero, G. González de Rivera y E. Juárez. "Introduction to LCA's Design" (In spanish). *ETSI Telecommunication Publication Service.* Technical University of Madrid, 1993.

Eduardo I. Boemo

Eduardo I. Boemo received the E.E. degree from the UNMdP (Universidad Nacional de Mar del Plata) of Argentina in 1985. Currently he is finishing the Ph.D. degree at the Universidad Politécnica de Madrid (UPM). From 1985 to 1987 he was an Assistant Professor of the Dept. of Physics (UNMdP). In 1988 he was a Visitant Researcher at the UPM. Since 1989 he is an Associate Professor at the School of Telecommunication (UPM) where he is in charge on Educational Laboratories at the Electronic Engineering Dept. As a consultant, he has participated on over a dozen of industrial projects on the VLSI and Communication areas. His current research interests include VLSI Array Processing, Computer Arithmetics, CAD Tools and E.E. Education. He has written 15 published papers, 3 technical books and has a registered patent on Computer Security. He has been Sponsoring Professor of the design winner of the 1992 Motorola University Design Contest, Zone Europe.

Juan M. Meneses

Juan M. Meneses received the Engineer degree and the Ph.D. degree both in Telecommunications, in 1977 and 1985 respectively by the Technical University of Madrid. At present the is Professor at the Electronics engineering Department of this University. This research activities are focused in: High speed architectures for implementing digital signal processing algorithms (speech and images applications) in real-time high-level synthesis methodologies for electronic design and its implementation. During these years he has been involved in research and development related with the topics above mentioned as director of a group of ten scientists. He has written more 25 published papers and four technical books in electronics engineering.