Computer-Based Tools for Electrical Engineering Education: Some Informal Notes

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Abstract: This paper proposes some ways to implement a modern Laboratory of Digital Electronics, suitable for universities situated in countries with incipient semiconductor industries and markets. It is focused on the areas of Logic Design and ASICs/FPGAs, two courses that today must be present in any of E.E. or C.S. undergraduate program. An annotated list of *www* links containing EDA tools, textbooks and tutorials is included.

1. INTRODUCTION

The electronic design has evolved from an artistic activity to a highly automated and methodical task. The change has been fast: less than thirty years separate the hand-made i4004 microprocessor layout from VHDL models of a RISC machines, performed nowadays by undergraduate students as a homework. In this way, the title of this paper could be considered redundant: a *non* computer-based E.E. education sounds today quite suspicious.

The increasing popularization of VLSI technology forces to separate the teaching of digital electronics in at least two parts: Logic Design, to embrace the fundamentals of digital circuits, followed by an ASIC Design course, to emphasize some aspect related to the circuit size (high-level description, complexity, synchronization, design automation, testing, cost, etc.). The second course requires selecting a given VLSI technology and its associated EDA tools to allow the student to practice the ASIC design cycle at the lab. In Table I is summarized the contents of such course, meanwhile the differences and synergy between the both courses is depicted in Table II.

ASIC Design can be oriented to Cell-based technologies (Standard Cells, Gate Arrays, SOGs, etc) or FPGAs. The first option has been described in several works [1]-[6]. Its most important drawback is the complexity of the tools [7] and the high cost of prototypes samples, even for educational prices [8], [9]. On the contrary, FPGA-based courses offer the professors several advantages: PC-based tools, free EDA tool licenses, a fast design cycle, and the reusability of the chip samples. Some references to this type of courses are [10]-[14]. Main problem of FPGAs is that the fixed structure of the chips and the use of LUTs instead of gates mask several VLSI details. In this way, a mixed approach can be the best option: to complement practical design using FPGAs, with some more theoretical chapters dedicated to Cell-based technology. It allows the professor to illustrate aspects like clock distribution, testability, load driving, optimization at gate-level, etc. Example of such courses can be found at [15], [16].

For several years, few instruments were utilized in educational laboratory to design and construct electronic systems. Typically, a DC power supply, an oscilloscope, and a signal generator were enough. Nowadays, the incorporation of ASIC design has appended expensive and ephemeral

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elements: powerful personal computers (or even workstations) as well as a set of licenses of EDA tools to specify, simulate and synthesize the circuits. They added new inconveniences to the classical labs problems, that can be summarized in the following points:

- Professional EDA tools are complex and can be plagued of bugs. Meanwhile the lab professors try to fix them, two or three new versions of the software can arrive at their desks.
- New tools naturally must to follow the Moore´s Law. Thus, more and more complex systems can be designed, but the cost is a higher and higher computing requirements. As consequence, the use of updated tools requires an unaffordable rate of renovation of the laboratory equipment.
- Current laboratory instruction requires three different types of vigilance that involves extra personnel and materials: a) a logical vigilance based on a PC network and a system manager to guarantee the SW integrity; b) an academic vigilance to avoid that a simple *diskcopy a: b:* (or similar) allows some students to significantly reduce the lab effort; and finally, c) ordinary vigilance to guarantee the lab integrity itself.

As a consequence, the installation, maintenance and day-to-day activities of a modern laboratory require a full dedication. Professors involved in these tasks are usually overcome by the problems and must to stop publishing papers during each laboratory semester. The long terms consequences of this fact have been pointed in some papers [17], [18].

2. UPGRADING EDUCATIONAL LABORATORIES: AN OPTIMISTIC APPROACH

Even considering the heavy arguments that usually persuade the prudent professors to avoid any change in educational laboratories, new facts are emerging to defense a policy of periodical updates. Some of these are:

- In the Internet age, tools, data books, manuals, and application notes are available from company websites. This is a definitive advance for all universities situated far from the semiconductor industries or markets. The popularization of CD ROMs also has contributed to make technical information more available.
- In the same direction, an impressive amount of educational material, product of long-hours of work and several years of classroom experience is available on Internet. The wide range of schools, campus and teachers guarantee the variety of this virtual catalog, where is almost impossible search no books, tools, exams, slides, etc. adequate for a particular course.
- Big semiconductor companies realized that they sell components, not software. A direct consequence of this fact is that today they are offering free powerful design tools.
- On the contrary, EDA companies, that precisely sell software, can not give its product free. However, the enormous competition for a market share moves these companies to offer evaluation versions of their tools, sometimes with limited features for industrial projects, but still enough useful for educational purposes.
- Engineering schools are recognized as key centers for the advertisement of both silicon and tools. Future graduates will probably select or recommend the products that they have used in the lab. In this way, several important companies maintain complete university programs

that give support to educational laboratories through donation or important discounts on samples, demonstration boards, courses, tools, etc. See as example [19].

- Meanwhile global industries requires the ultimate tools and silicon to create new products, skilled professors sometimes can transmit knowledge and methodology even using old-fashioned equipment. As an extreme example, most of the goals summarized in Table I (except VHDL) could be covered using the ten-year-old 1989 version of the Xilinx tools (e.g.: the *Futurenet-Xact-Silos* combination). This software run under DOS on 16-MHz PC AT 286´s with 4-MB RAM and a 20-MB hard disk, a configuration that today can be found only in Tech Museums. The 1999 equivalent tool (Foundation 1.5i) needs at least a 120-MHz Pentium Processor with 48-MB of free RAM and 2-GB hard disk [20].

Theme	Concept to learn
Hierarchical design	Decomposition in modules to simplify the implementation processes, and increment both design understandability and reusability.
Testability	The usefulness of extra elements to make possible the verification of the system.
Synchronization	Clocking and synchronous design principles. The tricks to be avoided.
Pipelining	The most direct way to speedup a circuit.
Physical design	The limitation of EDA tools, and the beneficial influence of an experienced designer.
VHDL (or Verilog)	The definitive advantages of a high-level language description to construct, document, or simulate an electronic system.
Area-time-power-design time trade-offs	The dialectic between these variables in any ASIC project. Different options at the architectural definition, the high-level description, and the physical design.
Algorithms for the Electronic Design Automation.	The fundamentals of the automatic implementation process and some hints to improve it.
Managing complexity	The appearance of problems related to the circuit size. The advantages of regularity.
Learning curve	The feeling that unknown tools can be learned and bugs can be exorcised. The knowledge of that the second and third pass throughout the design cycle will be performed really fast. The development of the student's self-confidence.
Economical factors	The technical fundamentals of IC´s costs, and the distortions that introduce the marketing activities.
Project documentation	The generation and organization of concise technical information.

Table I: Some goals for an FPGA /ASIC Design Course.

3. A LIST OF EDA TOOLS, TEXTBOOKS, AND TUTORIALS

In this section, a set of elements to configure an ASIC Design Lab is presented. The proposed course is based on FPGA technology and VHDL. Complementary alternatives for introductory laboratories (PALs) and advanced topics (Full-custom) are also included. All the required tools, documents and information are available on Internet: some of them are free, other offers educational prices and some of them can be downloaded just for evaluation. Several sites require a previous registration.

Feature	Logic Design		ASIC Design	
Problem size	10-100 gates	Basic designs using few standard modules: multiplexers, counters, coders, memories, etc.	5K-10K gates	Complex designs: algorithms to silicon, arithmetic blocks, small microprocessors, DSP parts, highly parallel circuits, Hw-Sw co-design, etc.
Level of abstraction	Low	Gates, AND-OR structures like PDLs.	High	Gates, Parameterized modules, IPs, VHDL models.
Complexity	Low	Few TTL-like component.	Medium-High	Heterogeneous circuits (e.g.: microprocessors). Combination of diverse modules and functions.
Background knowledge required	Low-none	Some basic ideas of Physics. A self-contained course on Logic Design can also be designed.	Medium-High	Design problems need to be complex. Students should have previous courses on Logic Design, Computer Architecture, Communication Systems, etc. in order to extend the scope of the lab exercises.
Design style	"Pencil and paper". TTL style.	Manual optimization of the circuits. Use of a logic simulator.	Exhaustive use of EDA tools.	Several mechanical aspects of the design are omitted. Use of logic modules as back-boxes. The description level is as high as possible. The emphasis is centered in the "productivity".
Design platform	Basic lab instruments.	The circuit size is limited by the problems inherent to the manual interconnection of discrete components.	Basic instruments plus a PC network. Licenses of professional EDA tools.	A fast design cycle based on specification-compilation-simulation.
Area-Time-Power details	Low	Wiring delay is neglectable. The concept of logic depth. Size refers to chip count.	Primary	Wiring delay is the central problem. Concepts of setup, hold, skew, global-local interconnection, throughput, etc.
Electronics details	Low	Limited to few concepts like open collector, three-state, pull-up, and fan-out.	Fundamental	Fanout-delay, deration with temperature, driving, clocking, synchronization, low-power design options, etc. Component of the chip area, I/O multiplexing, area-time overhead produced by a higher design specification level.
Bibliography	Elaborated and didactics	Textbooks, Book of solved exercises.	Raw information.	Databooks, Application Notes, Technical Papers, Tool manuals.
Organizational details	Simple	Lots of student can follow the course.	Complex	Few tool licences. Bugs and installation problems limit the amount of students. Difficulties to distribute the technical information.

Table II: Synergy between Logic Design and ASIC courses**.**

3.1 FPGA and ASIC Design EDA Tools

The election of a particular FPGA technology is complicated. The two usual alternatives, Xilinx or Altera, offer different options. The first allows the student to perform a detailed analysis of the circuit characteristics (delays, critical paths, etc.) and includes interesting alternatives for manual placement. The second is a highly integrated tool, where the VLSI details are more hidden. The student usually learns the Altera package very fast. Considering the rapid change in both technology and marketing strategies, professors interested in FPGAs must periodically evaluate, via Internet, the conditions and educational proposals of the top companies. A selected list of useful links[1] is:

- *http://www.xilinx.com/* This company offers the educational community one of the most complete University Programs. The site is essential for any professor interested in developing an FPGA course.
- *http://www.altera.com/* Other unavoidable site. An evaluation version of the great Max-PLUS II software is now available.
- *http://www.actel.com/* Actel offers a complete suite of its FPGA design tools for *qualified designers*. A literature request form can be found in the site.
- *http://www.sidsa.es/fipsoc.htm* The first *System-on-chip* FPGA. It also includes a 8051-like microcontroller and analog cells.
- *http://www.optimagic.com/* Other FPGA companies and links can be consulted form this site. The site periodically publishes the FPGA ranking.
- *http://www.vantis.com/* This company embrace the former PAL-related products of AMD. In this site, a free version of the popular PALASM 1.5 program can be downloaded. This program can be used in a basic course to illustrated concepts of hardware description language. The program runs on virtually any PC.
- *http://www.atmel.com/atmel/products/prod180.htm* This site provides a set of tools for Atmel EPLDs.
- *http://www.nuhorizons.com*/ and *http://www.newark.com* Current prices of several FPGA models.
- *http://infopad.eecs.berkeley.edu/~icdesign/tools.html* Here is the Magic full-custom design suite developed by the group of John Ousterhout at the University of California at Berkeley. It can run on Linux. The popular SPICE simulator can be also downloaded from this site.
- *http://www.mrc.uidaho.edu/cgi-bin/w3-msql/vlsi/CADfree.html* An extensive list of free tools for microelectronics design. Maintained by the Microelectronic Research and Communications Institute (University of Idaho).

3.2 VHDL

Most of the VHDL product can be downloaded for evaluation. However, some companies are offering important discounts in educational licenses.

[1] Interested readers do not need to tap these address: an updated and more complete list of the links can be found at *http://www.ii.uam.es /~ivan/ sitios.htm*

- *http://www.synopsys.com/products/eval/eval.html* This company offer a evaluation version of the FPGA Express, one of the most powerful tool for VHDL and Verilog synthesis. The VHDL databook itself (in *pdf* format) is a very useful textbook.
- *http://www.aldec.com/* A fully functional simulator can be downloaded for 30 day evaluation. This tool is also included with the Xilinx Foundation Series.
- *http://www.veribest.com/vhdl.html/* A evaluation version of this complete simulator is available.
- *http://www.vhdl.org/* Other companies and links can be consulted form this site.

3.3 Books and classroom material

Books and manuals on microelectronic technology have a short live. In this way, the *e-books* are a solution for student and universities with limited budget.

- *http://www-ee.eng.hawaii.edu/~msmith/ASICs/HTML/ASICs.htm* Here is the www-version of the extraordinary book of J.S. Smith [21]. The site includes the complete text, figures (in *pdf* format), exercises, tools, etc. It is very interesting the detailed information about economical aspect of integrated circuits.
- *http://infopad.eecs.berkeley.edu/~icdesign/* This page corresponds to the book of J. Rabaey [22]. A complete set of useful slides, exercises, and design tools are available.
- *http://nppp.jpl.nasa.gov/asic/title.page.html* This is an interesting book from the NASA that cover most of the aspects related to managing and contracting ASICs.
- *http://www.sematech.org/* In this site, the famous *National Technology Roadmap for Semiconductors* (1997 version) can be consulted. A complete glossary of microelectronic terms is also included.
- *ftp://ftp.cs.adelaide.edu.au/pub/VHDL-Cookbook/* The "VHDL Cookbook" of Peter Ashender can be downloaded.
- *http://www-s.ti.com/sc/docs/psheets/pids2.htm* In this page, the students can consult any component datasheet as well as application notes corresponding of Texas Instrument (the web version of the classical yellow databooks).

3.4 On-line tutorials

- *http://www-cad.eecs.berkeley.edu/~jimy/classes/ee244/hw2/index.html* In this site, an interesting program to illustrate the Simulated Annealing algorithm (SA) is offered. The tool shows a simplified 100-cell chip layout where the user can try manual moves or apply SA or Mincut techniques. Some algorithm parameter also can be modified.
- *http://tech-www.informatik.uni-hamburg.de/applets/cmos/cmosdemo.html* This is an Java-based tutorial of the CMOS transistor and basic gates. The user can fix the logic levels and see the behavior of some gates and components.
- *http://www.ehu.es/~jtpolagi/inicio.htm* One of the most complete VDHL tutorial, developed by the group of Prof. Iñigo Oleagordía at the *Escuela de Ingeniería Técnica Industrial de Bilbao*. It is based on the Warp tool of Cypress. All texts are in spanish language.

- *http://www.vhdl-online.de/~vhdl/* Other VHDL Tutorial from U. Heinkel, T. Bürner and M. Padeffke of the *Universität Erlangen-Nürnberg*
- *http://www.vlsivie.tuwien.ac.at/mike/vhdl4fpga/* On-line VHDL tutorial oriented to FPGAs.
- *http://www.euitt.upm.es/taee/product.htm* TAEE is a biannual conference similar to CAEE. Its site offers a database with several educational programs presented in the conferences.

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References

[1] "Teaching and Research Initiatives in VLSI Design". (Special Issue on Education). *IEE Proceeding.* Part G. Vol.139. Nº2. April 1992.

[2] Ainslie P. et al, "An Industry-Sponsored Professional Development Course: Design for Automotive ASICs", *IEEE Trans. on Education*, Vol.37, Nº2, Aug. 1994.

[3] Bouldin, D. "VLSI Education: Past, Present and Future", *Proceeding 1992 IEEE Frontiers in Education*, pp.732-736, Washington. IEEE Press 1992.

[4] Chen, T. "From System Design to IC Design in 14 Weeks - Teamwork Makes it Possible", *IEEE Trans. on Education*, Vol.36, Nº1, Feb.1993.

[5] Serra M. et al, "New Advances in Microelectronics Education: A Canadian Model", *IEEE Trans. on Education*, Vol.36, Nº1, Feb. 1993.

[6] O´Keefe M, et al, "Introducing VLSI Computer-Aided Design into the EE Curriculum: A Case-Study", *IEEE Trans. on Education*, Vol.32, Nº3, Aug.1989.

[7] Guyot, A. "Can Training in VLSI Design Keep Pace with Technology Development", Proc. of Int. Conf. on Microelectronics 1992 (ICM'92), Tunisia, December 1992. Available at http://tima-cmp.imag.fr/Homepages/guyot/publications.html

[8] Tomovich, C. "MOSIS - A Gateway to Silicon", *IEEE Circuits and Devices Magazine*, March 1988.

[9] *http://tima-cmp.imag.fr/CMP/CMP.html*

[10] Boemo E. and Meneses J. "Learning VLSI using FPGAs", *Proc. 23rd Frontiers in Education Conference*, pp.422-425. New York: IEEE Press 1993.

[11] Nixon, M. "On a Programmable Approach to Introducing Digital Design", *IEEE Trans. on Education*, Vol.40, Nº3, Agosto 1997.

[12] Degen, G. y Morgida, M. "Using Programmable Logic Devices in Undergraduate Digital Design Courses", *Proceeding 1993 IEEE Frontiers in Education.* IEEE Press 1993.

[13] Hack, R. et al, "The Use of FPGAs in Teaching Advanced Digital Circuits", *Proc. 1994 ASSEE Annual Conf.* pp.2078-2081.

[14] Vassileva and Tchoumatchenko, "Practical experience in teaching computed-aided design of ASICs", *Proc. 1993 Euroasic Conference.*

[15] http://www.ii.uam.es/~ivan/temario.htm

[16] Haskard, M, "Low-Cost Hands-on Training on Microelectronic Technologies", *IEEE Trans. on Education*, Vol.36, Nº3, Aug.1993.

[17] Van den Bout et al, "The NCSU Design Center", *Proceeding 1992 IEEE Frontiers in Education*, Nashville, 1992.

[18] Ernst, "A New Role for the Undergraduate Engineering Laboratory", *IEEE Trans. on Education*, Vol.E-26, No.2, May 1983.

[19] Xilinx University Program, http://www.xilinx.com/programs/univ.htm.

[20] Xilinx Inc. *"Foundation Series 1.5i Install and Release Document"*, Dec. 1998.

[21] Smith M., *"Application Specific Integrated Circuits"*, Addison-Wesley Publishing Company, June 1997.

[22] Rabaey J., "Digital Integrated Circuits: A Design Perspective", Prentice Hall, 1996.