FIELD PROGRAMMABLE LOGIC IN EDUCATION: A CASE STUDY

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Abstract

This paper presents a new undergraduate laboratory oriented to digital circuit design training based on Field Programmable Gate Arrays (FPGAs). The target of the course has been to introduce concepts of ASIC design methodology using a low cost alternative and a design-oriented, hands-on learning approach. FPGAs have permitted us to implement a massive VLSI-like design course, not only for future specialists but also for all Electrical Engineering and Computer Science students. Nowadays, about 450 students in their third year attend the laboratory at the School of Telecommunications of Madrid, Spain.

INTRODUCTION

Engineering is the application of science, technology and economy to resolve a problem. Thus, the importance of laboratories during the formation period is unquestionable. The student is able to obtain experience about the design cycle by solving concrete problems in laboratory courses.

In the area of electronics, there are usually several practical courses with contents ranging from standard off-the-shelf components to VLSI design. Standard component laboratories are inexpensive, easy to manage, and suitable to deal with a great quantity of students. However, they have an inherent problem: the complication of mounting and debugging the board. Although making a circuit run is an unforgettable and important experience, the physical implementation establishes limits on the size of the exercises that the student can achieve during a semester. Hence, there is not enough time for the exploration or evaluation of interesting architectures like microprocessors, pipelined arrays or other complex circuits.

On the contrary, VLSI laboratories permit the students to design elaborate and

attractive circuits, as well as get to know modern, powerful tools. However, managing a VLSI laboratory is a complicated and time consuming task that requires intensive instructor dedication; the design cycle is long, even for Gate Arrays or Standard Cells technologies; and finally, CAD platform and test equipment costs are high. Consequently, these kinds of courses are usually limited to a small number of students.

The appearance of high density FPGAs has became an ideal solution for digital electronic courses: it reduces the conceptual and economic gap between the laboratories described above by introducing a natural intermediate step. The main characteristics of FPGAs, fast design cycle and reprogrammability, allows the instructor to manage a great number of students, as is usual in most standard component laboratories. On the other hand, the FPGA design flow permits exercising all typical stages of VLSI design and their interactions: specification, logic entry, logical simulation, place and route, post-layout simulation, fabrication, testing, and generation of documentation. From the point of view of methodology, FPGAs evidence the advantages of hierarchical, modular, regular, testable, and synchronous designs. Finally, programmable logic circuits have opened suggestive horizons where they are insurmountable: dynamic reconfiguration circuits and fast prototyping. Both applications by themselves justify the inclusion of programmable logic circuits in an E.E. curriculum.

CHARACTERISTICS OF THE COURSE

As some VLSI design techniques have been taken from software engineering, the teaching of electronics can also benefit from the evolution of software education, that emphasizes formal concepts and general programming methodologies rather than the teaching of a particular language. Following this line, our course tries to accentuate general design techniques, decoupled from a particular product. The extremely fast design cycle of FPGAs, permits the establishment of a heuristic design-learning approach where the students can rediscover basic concepts. It allows to balance a E.E. education usually based on analysis, by the promotion of design habit.

The course is oriented to the design of a complete system instead of a collection of small examples. The successful resolution of such a problem which involves different trade-offs, is a good exercise of analysis, knowledge, astuteness, and intuition. It gives students the useful information and skills required to understand and estimate the complexity of future VLSI designs. The laboratory attempts to reproduce an ordinary situation in the actual engineering world: to solve an unknown problem with an unknown tool (with inevitable puzzling error messages, mysterious bugs and labyrinth manuals). The development of this skill is one of the most valuable goals of the course. Students can experiment the increasing gap between draft design and implementation of complex, high-performance systems.

The topics covered in the classroom are listed in Table I. Text books are Boemo *et al* (1992), Brown *et al* (1992) and product manuals. The complementary sessions in the laboratory start with a tutored example of a 16-bit counter whose structure at gate-level, must to be a copy of the well-known TTL 74163. The goals are to force the designer to acquire experience with the Xilinx`s CAD tool and to permit a comparison in size, cost, performance, and design time with respec to the TTL solution. After finishing the learning part, the students must implement a particular circuit. This attempts to put them face-to-face with a complex problem that usually has potential regularity and modularity. Finally, the students are invited to propose other design problems or to test the equivalent Altera development tools.

Table I: Undergraduate Course: "Laboratory of FPGAs"

Introduction	Time-to-Market and Concurrent Engineering. The Sources of Errors on Electronic Design. Programmable Logic Circuits: Evolution and Revolution in R&D. Products and Companies. Impact on Design Methodology and Production.
Architectures	Switch CMOS. Look-up Tables. XC3000 Family: Internal Structure: CLBs, IOBs and Interconnection Resources. Skew and Clock Lines. Configuration. XC4000 and Flex 8000 Families.
CAD Tool	Top-Down and Bottom-Up Design. Schematics vs. HDLs. Software Structure. Synthesis, Partitioning, Placement and Routing. CAD Algorithms. Module Generators. Xilinx XACT.
Simulation	Prelayout and Postlayout Simulation. Design for Testability: Observability and Controllability. Ad Hoc Techniques. Additional Logic for Testing. Scan Path.
Design I	Hierarchy. Synchronous Design. FPGA-Structure Oriented Designs. I/O. Routing Strategies. Including PALs. Configuration: Serial, Parallel and Daisy-Chain.
Design II	Manual Placement. Pull-Up, Wire-And and Buses. Map-then-Merge and Merge-then-Map. High Speed Design. Pad or Core Limited Circuits. Encapsulates and Electrical Characteristics.
Computer Arithmetic	Adders. Multipliers: Wallace, Booth, Dadda and Iteratives. Pipelining. Systolic Arrays. Skewing and Deskewing Registers. Latency and Throughput. Cost Functions. Bit-Serial Arithmetic. Self-Timed Circuits.
Conclusions	XC3000 vs. XC4000. FPGAs vs. Standard Cells. APR vs. CLBMAP+AR. PREP Benchmarks. Independent Vendors Tools. Perspectives.

SOME EXERCISES SUITABLE FOR A FPGA LABORATORY

The main advantage of FPGAs over standard off-the-shelf components is the possibility of building them in less time, more complex, reliable, and inexpensive electronic prototypes. The software-like design cycle permits the student to solve the same problem several times adopting different trade-offs. Principal guidelines for exercises used in a FPGA based laboratory are:

Computer Arithmetic: FPGAs have permitted to virtually everybody a way to design specific circuits in order to transfer algorithm to hardware. As a consequence, it has produced a renovated interest on computer arithmetic, whose principal ideas date from the '60s. Using FPGAs students can implement multipliers, adders, bit-serial circuits, etc. as well as to study some classical aspects like area-time trade-off, regularity, and extendibility of each solution.

Design of Microprocessor: Traditionally training on uP has been based on the use of a particular family of circuits. Today it is possible to update the E.E. curriculum by including some topics about designing uPs. Small processors with reduced set of instructions can be easily implemented using FPGAs. Some useful examples are More *et al* (1992), Grunbacher and Eder (1992), and Gal *et al* (1992).

Module Generators: Using Xilinx it is possible to synthesize circuits starting from the *xnf* or from the *map* format if some partitioning and placement strategies want to be added. Thus, students can design module generators for counters, adders, multipliers or other regular structures, and then integrate the resulting file in the standard design flow. Additionally, the knowledge of these formats is a interesting problem of reverse engineering. Using Altera`s FPGAs, the students can design module generators with the AHDL (Altera Hardware Description Language).

Pipelines and Systolic Arrays: The use of FPGAs with a great quantity of registers permits the implementation of pipelined circuits as well as bit-level systolic arrays. Thus the inherent speedup and hardware overhead of these techniques is understood. In the same way, the self-timed design approach can be introduced. Computer arithmetic circuits are again an inexhaustible source of exercises. As an example, an 8x8 bit systolic multiplier implemented with a XC3090PC84-100 occupies 235 CLBs and has throughput of 40 MOPS.

Design for Testability: FPGAs are tested devices and no fault simulation is necessary. However, the main DFT columns, observability and controllability, are fundamentals on FPGA design. It is possible to introduce some ad-hoc techniques in order to simplify circuit testing, like splitting counters, including a system reset signal, adding external control signals or checking incompatible combination of signal values. Students can learn about Scan Path or BILBO techniques by implementing case-study circuits on FPGAs. In resume, although testing is strongly coupled with a high density IC design, some of the themes about DFT teaching (Serra 1989, Absher 1991) can be sustained by a FPGA based laboratory.

CAD Tool Benchmarking: Students can test the ability of the standard tools, implementing the same circuit with different strategies: automatic placement and routing, using directives or performing a manual placement. Simulations and XACT are suitable to perform fast comparisons.

FPGA LABORATORY ORGANIZATION DETAILS

In the start-up stage, a scaled strategy was adopted. It was initiated with an experimental course with 20 selected students. It permitted us to detect some bugs and evidenced the necessity of a self-learning tutorial in order to manage the great amount of information in the data books. Next, experiments were carried out with 4 successive courses of 100 students each. In order to reduce laboratory maintenance costs, a set of security PC resident routines were developed. It permitted us to maintain the software uncorrupted, by preventing errors, viruses or vandal acts. Technical details of this program are reported in Boemo *et al* (1993).

The average learning response was measured to be about 15 hours for the tutorial. Currently, the laboratory is organized in an open door fashion, 12 hours/day from Monday to Friday, and 3-hour long sessions, with 20 Xilinx + 2 Altera design stations. For a 450 student course (the laboratory is compulsory for all students of the school), this configuration allows us to assign 26 hours/month per group (the work is done in groups of two). The short instruction time and the fast design cycle enables us to schedule two months for the FPGA course, and then continue with the complementary part of our laboratory (design of a microprocessor controlled systems).

Based on the supposition that PCs and software can be utilized for three years, the cost per student of the training is about 30 ECUs (it does not take into account professor and assistant costs). This is an incredible price for an ASIC-like course. Note on the other hand, that the amortization period is quite conservative; although fitting and routing algorithms are being improved every day, the concept involved in the design methodology will continue invariably. The use of non-updated software tools will not have serious educational consequences.

CONCLUSIONS

The results of the FPGA course have been highly positive. The students' response has been very enthusiastic and they have spent a lot of time in the laboratory. Some of the principal designs presented have been: frequency multipliers, arithmetic logic units, time-of-day clocks, microprocessors parts, fast counters, static ram memories, bit-level systolic arrays, FIR filters, bit-serial arithmetic circuits, several module generators for counters, decoders, state machines, shift registers and adders, and finally, a great variety of multipliers.

The first laboratory was started in 1990, and to this day it is completely stable. This course has also been successfully included in our continuing education program oriented to secondary school professors. The impact of the FPGA undergraduate laboratory over the promotion of the VLSI activities of our Department will be evaluated in a few years.

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