# A TEACHING EXPERIENCE ON VLSI DESIGN AT THE TECHNICAL UNIVERSITY OF MADRID

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**Abstract**

Undergraduate courses on Microelectronics are traditionally based on the study of circuits design, algorithms, device physics and technology. Nowadays, in spite of the cost of VLSI design and CAD tools it is necessary to add courses that emphasize the experience with current VLSI design tools. This paper describes the results of the teaching experience of the VLSI design laboratories at School of Telecommunication Engineering - Technical University of Madrid, Spain. This program is supported by EUROCHIP.

## I. Introduction.

The undergraduate VLSI design program at the ETSIT-UPM started in 1983. Although some prototypes were fabricated, most of the exercises were usually constrained to theoretical aspects due to the high cost of CAD tools and fabrication support. This situation changed drastically since the Eurochip initiative. Presently, a complete specialization (Area VI) exists on Microelectronics, within the Telecommunication Engineer Degree. The program has been focused on IC design and CAD and also includes many other courses covering fabrication processes, materials and devices. All the theoretical courses have a duration of 4-5 months (around 60 hours per course). The laboratories offer the student the possibility of getting practical experience on different topics related to the IC design. In the 6th year, the Final Project (M.Sc. Thesis) gives the opportunity of specialization on a wide variety of topics like Architectures, CAD, Reverse Engineering or Full-custom. These works are usually linked to research activities of our Department and require a at least 20 hours/week, during a minimum of 8-12 months of work.

## II. Engineering curriculum.

The common courses (taken by all the students) on electronics at the ETSIT-UPM are listed in Table I. Most of them have a compulsory laboratory course. Table II shows the specific courses on Microelectronics and CAD and in Table III the laboratories. Additionally, there are optative courses as Computers II, Computer Architecture, Digital System II, Operating Systems, Databases, System Engineering, Solid-State Physics, Semiconductors, Electronic Materials and Electronic Technology.

| | | |
|---|---|---|
| **2nd year** | Electronic Devices | Diode, Bipolar, JFET and MOS Transistor. Other devices. Amplifiers, ... |
| **2nd year** | Programming | Structured programming. Pascal. |
| **3rd year** | Integrated Circuits | IC fabrication. Physical and chemical processes. Digital and analog IC's structures. |
| **3rd year** | Digital Electronics | Gates, MSI, LSI, memories. Combinational and sequential logic. Finite state machines, ... |
| **3rd year** | Introduction to Computer I | Principles of computers. |
| **3rd year** | Digital Systems I | Principles of microprocessors. The 68000 Family. |
| **3rd year** | Linear Systems | Sampled and continuous, Laplace, Fourier and Z transformrs. |
| **4th year** | Electronics Circuits | Linear and analog circuits. Power amplifiers. Feedback. Frequency response ... |

Table I: Common courses on electronics

| | | |
|---|---|---|
| **4th year** | Microelectronics I | Models of Bipolar, JFET and MOS Transistors. Basic Blocks for analog IC's. |
| **5th year** | Microelectronics II | NMOS and CMOS fabrication process. Geometrical design rules. Layout. Electrical parameters restrictions. Scale down of design rules. Clocking. Testing. I/O. Packaging. Floorplanning. VLSI systems. Other CMOS design methodologies. Bipolar and high speed technologies. |
| **6th year** | Computed Aided Design | Basic algorithms and tools for the design of IC's. Databases, formats, user interfaces. Simulators. Tools for layout edition. Tools for test. Module generators. Silicon compilation. |

Table II: Courses on Microelectronics and CAD

The equipment and software of the Microelectronic laboratory is composed by five SUN SPARC stations (SPARC STATION 2, IPC, 1+ provided by EUROCHIP). All of them run CADENCE (SOLO2030). Moreover, there are six SUN 3 stations running only SOLO1400. There is also a TEXTRONIX LV500 testing station, linked with all the SUN SPARC stations by an ethernet network (TCP/IP). It allows to use the TEKWAVES software in order to test the design remotely.

In 1990, the design with FPGA was included at the third year course. It was decided in order to introduce the VLSI thematic to all students, in spite of the selected specialization of telecommunication engineering. One of the aims was to offer an attractive course to promote the microelectronic area. The election of the XC3000 family of Xilinx was motivated by the reasonable cost of software and platforms (PC AT and 386), suitable to deal with a great number of students (450 / year). A PC security software [1] was developed to permit:

- To establish passwords, system manager and account system.
- To avoid the execution of "dangerous" commands (like *format*).
- To avoid the change of any configuration file.
- To inhibit the booting process from *Drive A:*
- To restore the PC setup.
- To avoid the copy of user files.

A complete report of the final results can be found in [2].

| | | | STUDENTS/YEAR | LECTURERS |
|---|---|---|---|---|
| **3th year** | Digital Systems I | FPGA (XILINX) | 450 | 3 |
| **4th year** | Microelectronics I | PSPICE | 35 | 1 |
| **5th year** | Microelectronics II | Digital Design (Solo 1400, Cadence) | 18 | 1 |
| **5th-6th year** | Final Project | Full-custom, Reverse engineering, VHDL, Verilog, ... | 10 | 10 |

Table III: Laboratories on Microelectronics.

## III. Objectives of VLSI Courses.

The complexity and difficulties inherent to VLSI design can just be asimilated solving a design case. The use of actual tools (with its inevitable puzzling error messages, mysterious bugs and uncomplete manuals) is an instructive and unforgettable experience. The successful resolution of a problem is a good exercise of knowledge, astuteness and intuition and gives the students useful information and skill to understand and to estimate the size of future VLSI designs.

The goals of the course were to present the principal concepts, methodologies and problems that are common to every VLSI design, with independence of the tools used. The principal targets were:

- To practise with all the stages of design and their interactions: specification, logic entry, simulation, place and route, design rule checking and fabrication.
- To emphasize concepts of hierarchy, modularity and synchronous and testable designs.
- To learn to avoid complexity or sophistication.
- To generate complete and well-written documentation and reports.
- To learn how to manage and to estimate VLSI complexity.

Finally, the courses try to encourage the skill and training to use unknown tools, as it is a routine in R&D engineering laboratories.

## IV. Organization.

The laboratory was organized in an "open door" fashion. The students had access to the lab since 9 a.m. to 10 p.m. There was no negative consequence due to this policy. A system manager was in charge of all the maintenance, updating and distribution of resources, assisted by a technician. The academic responsibility was carry out for one professor and two lecturers.

Three kind of students use the laboratory: Ph.D. and Final Project applicants, and Microelectronic's students. The last ones join groups (2 or 3 student/group) in order to share the scarce resources and to stimulate working as a team and to make easier the resolution of the different problems that arise during the work. The cooperation spirit among all the students has allowed them to solve every gap between the tools and manuals. All together worked as a "user group".

One of the projects proposed last year was a binary multiplier. It has many characteristics that make it suitable for the course: easy to understand, regular architecture and lots of technical literature. It makes possible to compare its performance with many commercial versions [3]-[6], previous results obtained with FPGA [7] or with other similar VLSI educative initiatives [8]. The best design was fabricated and reported in [9]. On the other hand some students proposed to design their own circuit.

The main undergraduate designs were:

- 8-Bit Binary Multiplier.
- Chronometer/Tachometer
- Programmable Digital Filter (FIR and IRR).
- Bit Slice (2901 architecture).

## V. Final Project new lines.

On June 1991, a small group of student went on the training making their Final Projects with the design of a novel architecture for Speech Recognition [10] based on Hidden Markov Models (HMM) [11]. The chip designed implements the Viterbi Algorithm over HMM's (from now onwards named Viterbi Processor, results were reported in [12]), being the main factors involved the following:

- Speaker Independence.
- Large Vocabularies (up to 3000 words).
- Real-Time.
- Isolated utterance.
- Highly pipelined architecture [13].
- Internal parallelism.

To get maximum efficiency using the least number of gates and silicon area have been the main design goals. Main lines of research that has been followed are:

- Versatility: Adapting the chip architecture in order to support different HMM's (3 or 5 states and 2 or 3 transitions per state).

- Flexibility: The Viterbi Processor uses a Control Unit running a set of programs stored into a PLA. Its functionality is equivalent to a microprogrammed control unit.

- Modifying the Algorithm to decrease computational load and silicon area.

- Non Overlapped Two Phases Clock System: One phase controlling the Control Unit (marking processor states) and the other controlling the rest of the Processor.

- Pipelined Architecture: Maximal throughput have been reached using analysis techniques for its control, described in [13], in spite of the HMM used.

The physical design has been done with SOLO2030 (since June 1991 until July 1992) and the main characteristics are:

- Technology: Semicustom CMOS, 1.5 microns
- Clock Frequency: 25MHz.
- Overall chip area: 78,04 $mm^2$
- Approximate number of transistors: 34120
- Test structures: BIST (for internal RAM)
- Pinout: 128
- Package: PGA (144 pins)
- Vocabulary length: 1020 words at 25MHz
- MPC run: 1st of September

As a result of this experience, a new student started out his Final Project on March 1992 until July 1992. The main target of this Project was to design a chip to improve the Viterbi Processor performance and applications. This chip is a Finite State Machine (FSM) that allows continuous speech recognition (Grammar Processor). It works during the elapsed time where the Viterbi Processor is idle (between two consecutive words to be processed). The main characteristics of this design are:

- Technology: Semicustom CMOS, 1.5 microns
- Clock Frequency: 25MHz.
- Overall chip area: 22,06 $mm^2$
- Approximate number of transistors: 5266
- Test structures: None
- Package: PGA (120 pins)
- MPC run: 1st of July

Both design will be presented at Poster Sessions, Third Eurochip Worshop on VLSI Design Training.

## VI. Conclusions and Comment

The possibility of designing and fabrication their own circuit was very exciting for the students. They worked very motivated and stayed a lot of time in the laboratory.

The main problems and start-up mistakes of our laboratory are probably very common and were also reported in other VLSI teaching papers [8],[14]. Some students have failed due to a bad planning of their design time, so all the work was accumulated in the last weeks of the semester. To correct it, intermediate deadline will be state next course. On the other hand, the complaints were focused on the lack of clearness and completeness of CADENCE manual and reference guides.

Difficulty about design, manufacture and test a CI in an academic year suggests that it could be interesting to start the course with the testing of the prototypes fabricated the previous semester.

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