Motorola Semiconductor Engineering Bulletin

EB366

In-Circuit Programming of FLASH Memory Using the Monitor Mode for the MC68HC908GP32

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Introduction

This engineering bulletin describes how to perform in-circuit programming (ICP) of the FLASH memory using monitor mode for the MC68HC908GP32.

Two ICP methods are discussed here:

• Using the M68ICS08GP in-circuit simulator (ICS) with P&E Microsystems software
• Using P&E Microsystems software with an external communications circuit

ICP is a process where user code is programmed into the device’s FLASH memory after the part has been assembled into the application. ICP also allows the original users code to be erased and re-programmed. This method can be used in development, production/manufacturing, and in a field environment.
Using Monitor Mode for FLASH Programming

Motorola’s current solution for ICP is the in-circuit simulators and P&E’s software.

The software and ICS allow programming of the parts on the simulator or in the target circuit via a MON08 ribbon cable. The software also allows programming of the part, without the ICS, by using an external communications circuit.

All the programming described here is accomplished by placing the part into monitor mode. In this mode, erasing and programming are done through a single-wire interface with the host computer.

The two ways to enter monitor mode are:

- The ICS provides the entry requirements into standard monitor mode. These entry requirements must be implemented on the target board if the ICS is not used.
- A second way to enter monitor mode, that does not require a high voltage on the IRQ pin, is forced monitor mode. This mode does not need to meet all the monitor mode entry conditions of the standard monitor mode, but it does require the part to be blank (erased).

This engineering bulletin describes how to connect the part, communicate at different baud rates, place the part into monitor mode, pass security, and erase and program the part. If the security code is not known, the contents of the FLASH can’t be read, but the FLASH can be erased and reprogrammed.

Information on the M68ICS08GP can be found at http://mcu.motsps.com. P&E Microsystems software can be downloaded free from that company’s Web site.

**NOTE:** All of the oscillators used in this engineering bulletin are the 4-pin “powered” or “canned” type oscillators. Discussing all the different vendors of crystals, ceramic oscillators, other required external components, and component layout variables would be too extensive.
ICP Using M68ICS08GP's MON08 Interface

Use this procedure for performing ICP using the ICS's MON08 cable to the target application.

1. Materials required:
   a. PC with P&E’s software installed (version 1.32 or higher)
   b. M68ICS08GP simulator
   c. Adapter/connector to connect the female end of the MON08 cable to the target application
   d. Pin assignment diagram (see Figure 1, Figure 2, and Figure 3)
   e. Monitor mode entry requirements (see Table 1)
   f. Crystal oscillator on the target or from an external clock source with a value from Table 2
   g. Target board must have the ability to perform a power-on reset (POR) not just a reset (required to enter monitor mode).

2. Connections (see Figure 4):
   a. 9-pin serial cable from PC to the ICS
   b. 5 volts to the ICS
   c. MON08 cable (even pins) from J6 of the ICS to the target board with these connections:
      — MON08 GND to the VSS pin on the part
      — MON08 RST to the RST pin on the part
      — MON08 IRQ to the IRQ pin on the part
      — MON08 PTA0 to the PTA0 pin on the part
      — MON08 PTA7 to the PTA7 pin on the part
      — MON08 PTC0 to the PTC0 pin on the part
      — MON08 PTC1 to the PTC1 pin on the part
      — MON08 PTC3 to the PTC3 pin on the part
   d. It is assumed that all VDD and VSS pins on the part are already connected.
3. Operation — Standard monitor mode entry:
   a. Launch P&E’s WINIDE in the ICS08GPZ software.
   b. Open desired file. (Demo file can be used for testing purposes.)
   c. Assemble/Compile the file (see Figure 8).
   d. Plug in power to the ICS.
   e. Turn on power to the target.
   f. Launch the programmer.
   g. From “Target Hardware Type,” select “Class II” (see Figure 9).
   h. From “PC Serial Port Configuration,” select the PC port you are using and the appropriate baud rate (see Table 2).
   i. From “Target MCU Security Bytes,” select appropriate security code (blank part = FF).
   j. Select “Contact Target with these Settings…”
   k. Follow the instructions in the “Power Down/Up Dialog” windows.
   l. Select appropriate algorithm for the part. The high-speed algorithm will not work at 28,800 baud.
   m. Double click on “Erase Module” – EM (see Figure 10).
   n. Double click on “Program Module” – PM.
   o. Record security bytes. This information can be seen by quitting and then re-entering the programmer. The S19 record will have the same security bytes as the part just programmed as long as it is not changed. The security bytes consist of the information stored in the interrupt vectors, $FFF6–$FFFD.

4. Operation — Forced monitor mode entry:
   a. Forced monitor mode is not supported by this ICS. However, this mode can be entered by using the procedure found in ICP Using the External Communications Circuit (No ICS).
ICP Using the External Communications Circuit (No ICS)

Use this procedure for performing ICP via an external communications circuit in place of this ICS to the target application.

1. Materials required:
   a. PC with P&E software installed (version 1.32 or higher)
   b. Adapter/connector to connect the male end of the 9 pin serial cable to the target application
   c. The external communications circuit. Also needed is a 5-volt power source to power this circuit (see Figure 5, Figure 6, and Figure 7).
   d. Pin assignment diagram (see Figure 1, Figure 2, and Figure 3)
   e. Monitor mode entry requirements (see Table 1)
   f. Crystal oscillator on the target or from an external clock source, with a value from Table 2
   g. Target board must have the ability to perform a POR not just a reset of the part (required to enter monitor mode).

2. Connections (see Figure 5):
   a. 9-pin serial cable from PC to the external communications circuit
   b. V+ pin of the RS-232 part to the IRQ pin of the part
   c. Communication pin of HC125 to PTA0 of the part
   d. Target pin requirements:
      — PTA7 of the part to VSS
      — PTC0 of the part to VDD via a pullup resistor
      — PTC1 of the part to VSS
      — PTC3 of the part to VSS (crystal frequency ÷ 2) or VDD via pullup resistor (crystal frequency ÷ 4). See Table 2.
      — RESET has an internal pullup resistor.
   e. It is assumed that all VDD and VSS pins on the part are already connected.
3. Operation — Standard monitor mode entry:
   a. Launch P&E’s WINIDE in the ICS08GPZ software.
   b. Open desired file. (Demo file can be used for testing purposes.)
   c. Assemble/Compile the file (see Figure 8).
   d. Apply power to the external communications circuit.
   e. Turn on power to the target.
   f. Launch the programmer.
   g. From “Target Hardware Type,” select “Class III” (see Figure 9).
   h. From “PC Serial Port Configuration,” select the PC port in use and the appropriate baud rate (Table 2).
   i. From “Target MCU Security Bytes,” select appropriate security code (blank part = FF).
   j. Select “Contact Target with these Settings…”
   k. Follow the instructions in the “Power Cycle Dialog” window.
   l. Select appropriate algorithm for the part. The high-speed algorithm will not work at 28,800 baud.
   m. Double click on “Erase Module” – EM (see Figure 10).
   n. Double click on “Program Module” – PM.
   o. Record security bytes. This information can be seen by quitting and then re-entering the programmer. The S19 record will have the same security bytes as the part just programmed as long as it is not changed. The security bytes consist of the information stored in the interrupt vectors, $FF6–$FFFD.

4. Operation — Forced monitor mode entry:
   a. Blank part with oscillator value from Table 2. See Figure 6.
      — Remove connection to the IRQ pin from V+ of the external communications circuit.
      — No connections to PTC0, PTC1, and PTC3 are necessary in this mode.
      — IRQ has an internal pullup resistor.
   b. Blank part with a 32.768-kHz oscillator. See Figure 7.
      — Connect the IRQ pin to VSS.
Figure 1. 40-Pin PDIP Pin Assignments

NOTE: PTC5, PTC6, PTD6, and PTD7 were removed for this package.
Figure 2. 42-Pin SDIP Pin Assignments

NOTE: PTC5 and PTC6 were removed for this package.
Figure 3. 44-Pin QFP Pin Assignments
## Table 1. Monitor Mode Signal Requirements and Options

<table>
<thead>
<tr>
<th>IRQ</th>
<th>RESET</th>
<th>SFFFF/ SFFFFF</th>
<th>PLL</th>
<th>PTC0</th>
<th>PTC1</th>
<th>PTC3</th>
<th>External Clock(1)</th>
<th>CGMOUT</th>
<th>Bus Frequency</th>
<th>COP</th>
<th>For Serial Communication</th>
<th>Comment</th>
</tr>
</thead>
<tbody>
<tr>
<td>X</td>
<td>GND</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>0</td>
<td>0</td>
<td>Disabled</td>
<td>X</td>
<td>X</td>
</tr>
<tr>
<td>VTST</td>
<td></td>
<td>VDD or VTST</td>
<td>OFF</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>4.9152 MHz</td>
<td>4.9152 MHz</td>
<td>2.4576 MHz</td>
<td>Disabled</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>VTST</td>
<td></td>
<td>VDD or VTST</td>
<td>OFF</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>9.8304 MHz</td>
<td>4.9152 MHz</td>
<td>2.4576 MHz</td>
<td>Disabled</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>VDD</td>
<td>VDD</td>
<td>$FF$ (blank)</td>
<td>OFF</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>9.8304 MHz</td>
<td>4.9152 MHz</td>
<td>2.4576 MHz</td>
<td>Disabled</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>GND</td>
<td>VDD</td>
<td>$FF$ (blank)</td>
<td>ON</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>32.768 kHz</td>
<td>4.9152 MHz</td>
<td>2.4576 MHz</td>
<td>Disabled</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>VDD or GND</td>
<td>VDD</td>
<td>$FF$ (blank)</td>
<td>OFF</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>Enabled</td>
<td>X</td>
</tr>
<tr>
<td>VDD or GND</td>
<td>VDD</td>
<td>$FF$ (programmed)</td>
<td>OFF</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>Enabled</td>
<td>X</td>
</tr>
</tbody>
</table>

1. External clock is derived by a 32.768-kHz crystal or a 4.9152/9.8304-MHz off-chip oscillator.
2. PTA0 = 1 if serial communication; PTA0 = X if parallel communication
3. PTA7 = 0 → serial, PTA7 = 1 → parallel communication for security code entry
4. DNA = does not apply, X = don’t care
Table 2. Crystal Frequency vs Baud Rate

<table>
<thead>
<tr>
<th>Crystal Frequency (MHz)</th>
<th>Internal Bus Frequency (MHz)</th>
<th>Baud Rate</th>
</tr>
</thead>
<tbody>
<tr>
<td>2.4576</td>
<td>1.2288</td>
<td>4800</td>
</tr>
<tr>
<td>4.9152</td>
<td>2.4576</td>
<td>9600</td>
</tr>
<tr>
<td>7.3728</td>
<td>3.6864</td>
<td>14,400</td>
</tr>
<tr>
<td>9.8304</td>
<td>4.9152</td>
<td>19,200</td>
</tr>
<tr>
<td>14.7456</td>
<td>7.3728</td>
<td>28,800</td>
</tr>
</tbody>
</table>

Divide by 4 Option (PTC3 to VDD)

<table>
<thead>
<tr>
<th>Crystal Frequency (MHz)</th>
<th>Internal Bus Frequency (MHz)</th>
<th>Baud Rate</th>
</tr>
</thead>
<tbody>
<tr>
<td>4.9152</td>
<td>1.2288</td>
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</tr>
<tr>
<td>9.8304</td>
<td>2.4576</td>
<td>9600</td>
</tr>
<tr>
<td>14.7456</td>
<td>3.6864</td>
<td>14,400</td>
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<td>19.6608</td>
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<td>19,200</td>
</tr>
<tr>
<td>29.4912</td>
<td>7.3728</td>
<td>28,800</td>
</tr>
</tbody>
</table>

Figure 4. MC68HC908GP32 MON08 Connections
Figure 5. MC68HC908GP32 Standard Monitor Mode (9.8304 MHz)

Figure 6. MC68HC908GP32 Forced Monitor Mode (9.8304 MHz)
**Figure 7.** MC68HC908GP32 Forced Monitor Mode (32.768 kHz)

**Figure 8.** P&E’s WINIDE Window
Figure 9. P&E’s Target and Security Window
Figure 10. P&E's Programmer Window
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