19-2134; Rev 3; 1/08

SPI-Compatible RTC in a TDFN

General Description

The MAX6902 SPI™-compatible real-time clock contains a real-time clock/calendar and 31 x 8 bits of static random-access memory (SRAM). The real-time clock/calendar provides seconds, minutes, hours, day, date, month, year, and century information. A time/date programmable polled ALARM is included in the MAX6902. The end-of-the-month date is automatically adjusted for months with fewer than 31 days, including corrections for leap year up to the year 2100. The clock operates in either the 24hr or 12hr format with an AM/PM indicator. The MAX6902 operates with a supply voltage of +2V to +5.5V, is available in the ultra-small 8-pin TDFN package, and works over the -40°C to +85°C industrial temperature range.

Applications

Point-of-Sale Equipment

Intelligent Instruments

Fax Machines

Battery-Powered Products

Portable Instruments

Features

- **Real-Time Clock Counts Seconds, Minutes, Hours, Day of Week, Date of Month, Month, Year, and Century**
- **Leap-Year Compensation Valid up to Year 2100**
- **+2V to +5.5V Wide Operating Voltage Range**
- **SPI Interface: 4MHz at 5V; 1MHz at 2V**
- **31 x 8-Bit SRAM for Scratchpad Data Storage**
- **Uses Standard 32.768kHz, 12.5pF Watch Crystal**
- **Low Timekeeping Current (400nA at 2V)**
- **Single-Byte or Multiple-Byte (Burst Mode) Data Transfer for Read or Write of Clock Registers or SRAM**
- **Ultra-Small 8-Pin 3mm x 3mm x 0.8mm TDFN Package**
- **Programmable Time/Date Polled ALARM Function**
- **No External Crystal Bias Resistors or Capacitors Required**

Ordering Information

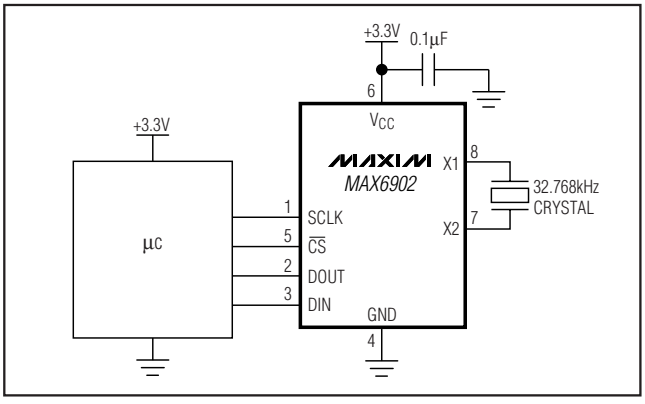
PART	TEMP RANGE	PIN-PACKAGE	TOP MARK
MAX6902ETA+T	-40°C to +85°C	8 TDFN	+AGT

+Denotes lead-free package.

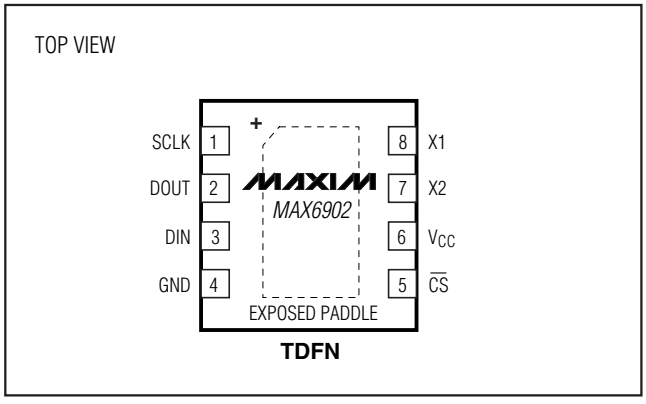
Related Real-Time Clock Products

PART	SERIAL INTERFACE	SRAM	ALARM FUNCTION	OUTPUT FREQUENCY	PIN-PACKAGE
MAX6900	I²C compatible	31 × 8	—	—	6 TDFN
MAX6901	3 Wire	31 × 8	Polled	32kHz	8 TDFN
MAX6902	SPI compatible	31 × 8	Polled	—	8 TDFN

Typical Operating Circuit



Pin Configuration



SPI is a trademark of Motorola, Inc.

FUNCTION CLOCK		REGISTER ADDRESS A7	A6	A5	A4	A3	A2	A1	A0	VALUE	REGISTER DEFINITION D7	D6	D5	D4	D3	D2	D1	D0
SECONDS	RD	0	0	0	0	0	0	1		00-59	0	10 SEC			1 SEC			
	/W									*POR STATE	0	0	0	0	0	0	0	0
MINUTES	RD	0	0	0	0	0	1	1		00-59	ALM OUT	10 MIN			1 MIN			
	/W									*POR STATE	0	0	0	0	0	0	0	0
HOURS	RD	0	0	0	0	1	0	1		00-23	12/24	0	10 HR	10 HR	1 HR			
	/W									01-12	1/0		A/P 0/1					
										*POR STATE	0	0	0	0	0	0	0	0
DATE	RD	0	0	0	0	1	1	1		01-28/29 01-30 0-31	0	0	10 DATE		1 DATE			
	/W									*POR STATE	0	0	0	0	0	0	0	1
MONTH	RD	0	0	0	1	0	0	1		01-12	0	0	0	10M	1 MONTH			
	/W									*POR STATE	0	0	0	0	0	0	0	1
DAY	RD	0	0	0	1	0	1	1		01-07	0	0	0	0	0	WEEK DAY		
	/W									*POR STATE	0	0	0	0	0	0	0	1
YEAR	RD	0	0	0	1	1	0	1		00-99	10 YEAR				1 YEAR			
	/W									*POR STATE	0	1	1	1	0	0	0	0
CONTROL	RD	0	0	0	1	1	1	1			WP	0	0	0	0	0	0	0
	/W									*POR STATE	0	0	0	0	0	0	0	0
CENTURY	RD	0	0	1	0	0	1	1		00-99	1000 YEAR				100 YEAR			
	/W									*POR STATE	0	0	0	1	1	0	0	1

Note: *POR STATE defines power-on reset state of register contents.

Figure 2. Register Address Definition (Sheet 1 of 3)

SPI-Compatible RTC in a TDFN

FUNCTION		REGISTER ADDRESS A7	A6	A5	A4	A3	A2	A1	A0	VALUE	REGISTER DEFINITION D7	D6	D5	D4	D3	D2	D1	D0
ALARM CONFIG	RD	**0**	**0**	**1**	**0**	**1**	**0**	**1**			0	YEAR	DAY	MONTH	DATE	HOUR	MINUTE	SECOND
	/W									***POR STATE**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
RESERVED Do not write to this location.	RD	0	0	1	0	1	1	1			0	0	0	0	0	1	1	1
	/W									***POR STATE**	0	0	0	0	0	1	1	1
ALARM THRESHOLDS																		
SECONDS	RD	**0**	**0**	**1**	**1**	**0**	**0**	**1**		00-59	0	10 SEC			1 SEC			
	/W									***POR STATE**	**0**	**1**	**1**	**1**	**1**	**1**	**1**	**1**
MINUTES	RD	**0**	**0**	**1**	**1**	**0**	**1**	**1**		00-59	0	10 MIN			1 MIN			
	/W									***POR STATE**	**0**	**1**	**1**	**1**	**1**	**1**	**1**	**1**
HOURS	RD	**0**	**0**	**1**	**1**	**1**	**0**	**1**		00-23	12/24	0	10 HR	10 HR	1 HR			
	/W									01-12	1/0		A/P 0/1					
										***POR STATE**	**1**	**0**	**1**	**1**	**1**	**1**	**1**	**1**
DATE	RD	**0**	**0**	**1**	**1**	**1**	**1**	**1**		01-28/29 01-30 01-31	0	0	10 DATE		1 DATE			
	/W									***POR STATE**	**0**	**0**	**1**	**1**	**1**	**1**	**1**	**1**
MONTH	RD	**0**	**1**	**0**	**0**	**0**	**0**	**1**		01-12	0	0	0	10M	1 MONTH			
	/W									***POR STATE**	**0**	**0**	**0**	**1**	**1**	**1**	**1**	**1**
DAY	RD	**0**	**1**	**0**	**0**	**0**	**1**	**1**		01-07	0	0	0	0	0	WEEK DAY		
	/W									***POR STATE**	**0**	**0**	**0**	**0**	**0**	**1**	**1**	**1**
YEAR	RD	**0**	**1**	**0**	**0**	**1**	**0**	**1**		00-99	10 YEAR				1 YEAR			
	/W									***POR STATE**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**
CLOCK BURST	RD	**0**	**1**	**1**	**1**	**1**	**1**	**1**										
	/W																	

Figure 2. Register Address Definition (Sheet 2 of 3)

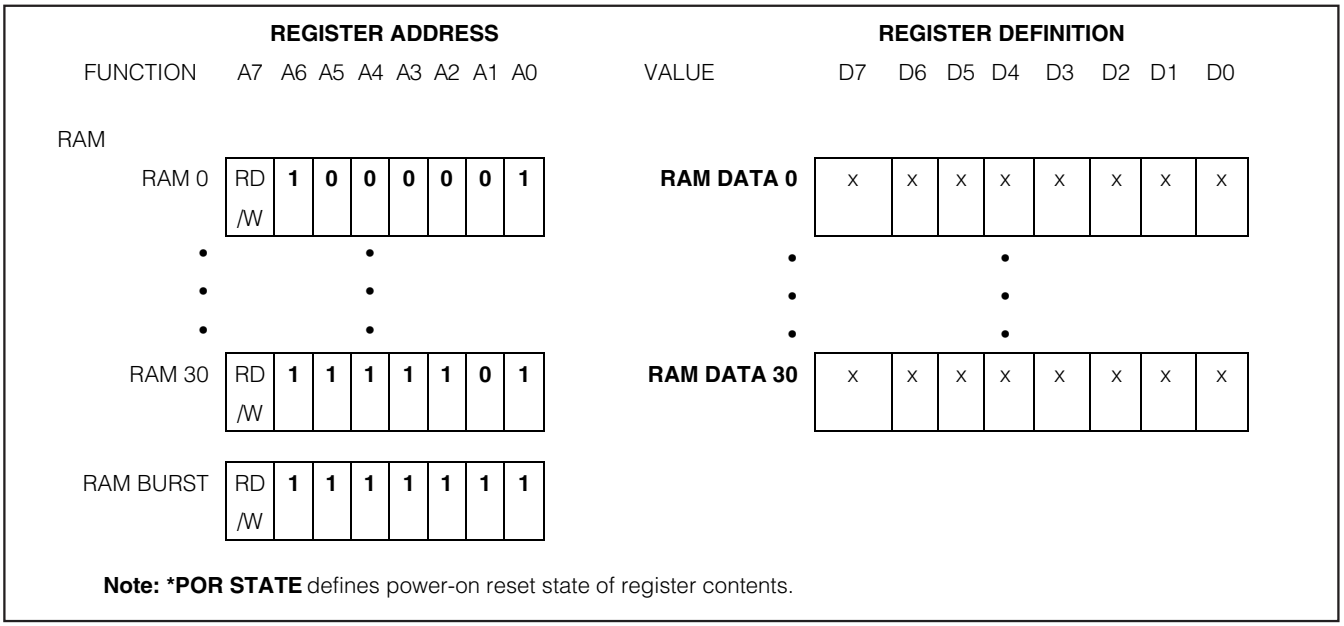


Figure 2. Register Address Definition (Sheet 3 of 3)

Table 2. Register Address and Description

WRITE (HEX)	READ (HEX)	DESCRIPTION	POR CONTENTS (HEX)
01	81	Seconds	00
03	83	Minutes	00
05	85	Hours	00
07	87	Date	01
09	89	Month	01
0B	8B	Day	01
0D	8D	Year	70
0F	8F	Control	00
13	93	Century	19
15	95	Alarm Configuration	00
17	97	Reserved	07
19	99	Seconds Alarm Threshold	7F
1B	9B	Minutes Alarm Threshold	7F
1D	9D	Hours Alarm Threshold	BF
1F	9F	Date Alarm Threshold	3F
21	A1	Month Alarm Threshold	1F
23	A3	Day Alarm Threshold	07
25	A5	Year Alarm Threshold	FF
3F	BF	Clock Burst	Not applicable

Table 2. Register Address and Description (continued)

WRITE (HEX)	READ (HEX)	DESCRIPTION	POR CONTENTS (HEX)
41	C1	RAM 0	Indeterminate
43	C3	RAM 1	Indeterminate
45	C5	RAM 2	Indeterminate
47	C7	RAM 3	Indeterminate
49	C9	RAM 4	Indeterminate
4B	CB	RAM 5	Indeterminate
4D	CD	RAM 6	Indeterminate
4F	CF	RAM 7	Indeterminate
51	D1	RAM 8	Indeterminate
53	D3	RAM 9	Indeterminate
55	D5	RAM 10	Indeterminate
57	D7	RAM 11	Indeterminate
59	D9	RAM 12	Indeterminate
5B	DB	RAM 13	Indeterminate
5D	DD	RAM 14	Indeterminate
5F	DF	RAM 15	Indeterminate
61	E1	RAM 16	Indeterminate
63	E3	RAM 17	Indeterminate
65	E5	RAM 18	Indeterminate
67	E7	RAM 19	Indeterminate
69	E9	RAM 20	Indeterminate
6B	EB	RAM 21	Indeterminate
6D	ED	RAM 22	Indeterminate
6F	EF	RAM 23	Indeterminate
71	F1	RAM 24	Indeterminate
73	F3	RAM 25	Indeterminate
75	F5	RAM 26	Indeterminate
77	F7	RAM 27	Indeterminate
79	F9	RAM 28	Indeterminate
7B	FB	RAM 29	Indeterminate
7D	FD	RAM 30	Indeterminate
7F	FF	RAM Burst	Not applicable

Using the On-Board RAM

The static RAM is 31 x 8 bits addressed consecutively in the RAM Address/Command space. Table 2 details the specific hex Address/Commands for Reads and Writes to each of the 31 locations of RAM. The contents of the RAM are static and remain valid for V_{CC} down to 2V. All RAM data are lost if power is cycled. The Write-Protect Bit (bit 7 of the Control register), when high, disallows any writes to RAM.

SPI-Compatible Serial Interface

Interface the MAX6902 with a microcontroller using a serial, 4-wire, SPI interface. SPI is a synchronous bus for address and data transfer, and is used with Motorola or other microcontrollers that have an SPI port. Four connections are required for the interface: DOUT (Serial Data Out); DIN (Serial Data In); SCLK (Serial Clock); and $\overline{CS}$ (Chip Select). In an SPI application, the MAX6902 acts as a slave device and the microcontroller acts as the master. $\overline{CS}$ is asserted low by the microcontroller to initiate a transfer, and deasserted high to terminate a transfer. DIN transfers input data from the microcontroller to the MAX6902. DOUT transfers output data from the MAX6902 to the microcontroller. A shift clock, SCLK, is used to synchronize data movement between the microcontroller and the MAX6902. SCLK, which is generated by the microcontroller, is active only during address and data transfer to any device on the SPI bus. The inactive clock polarity is usually programmable on the microcontroller side of the SPI interface. In the MAX6902, input data are latched on the positive edge, and output data are shifted out on the negative edge. There is one clock cycle for each bit transferred. Address and data bits are transferred in groups of eight.

The SPI protocol allows for one of four combinations of serial clock phase and polarity from the microcontroller, through a 2-bit selection in its SPI Control register. The clock polarity is specified by the CPOL Control bit, which selects active-high or active-low clock, and has no significant effect on the transfer format. The Clock Phase Control bit, CPHA, selects one of two different transfer formats. The clock phase and polarity must be identical for the master and the slave. For the MAX6902, set the control bits to CPHA = 1 and CPOL = 1. This configures the system for data to be launched on the negative edge of SCLK and sampled on the positive edge. With CPHA equal to 1, $\overline{CS}$ can remain low between successive data byte transfers, allowing burst-mode data transfers to occur.

Address and data bytes are shifted MSB first into DIN of the MAX6902, and out of DOUT. Data are shifted out at the negative edge of SCLK, and shifted in or sampled at the positive edge of SCLK. Any transfer requires an Address/Command byte followed by one or more bytes of data. Data are transferred out of DOUT for a read operation, and into DIN for a write operation. DOUT transmits data only after an Address/Command byte specifies a read operation; otherwise, it is high impedance.

Data Transfer Write timing is shown in Figure 3. Data Transfer Read timing is shown in Figure 4. Detailed Read and Write Timing is shown in Figure 5.

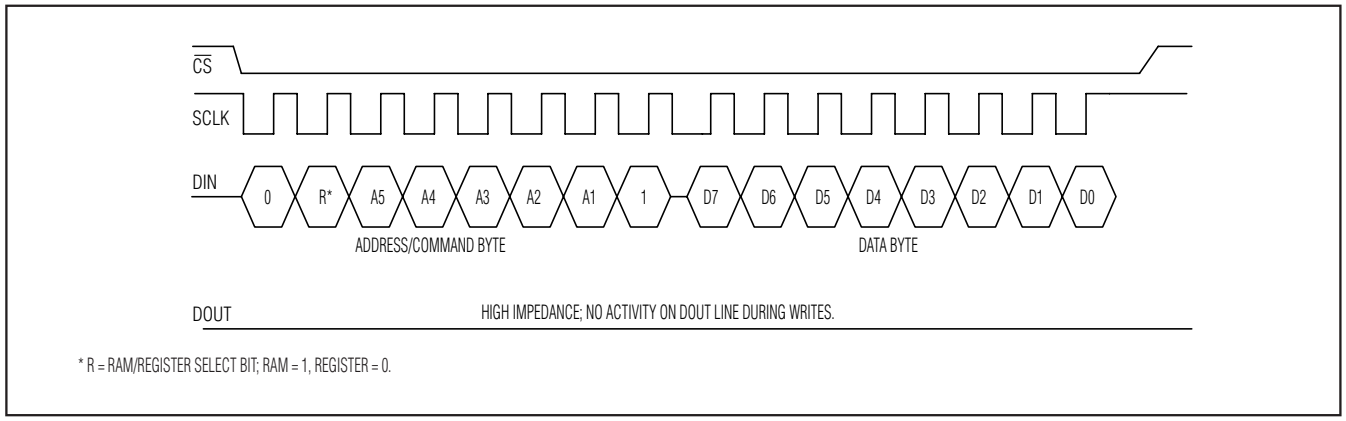


Figure 3a. Single Write

SPI-Compatible RTC in a TDFN

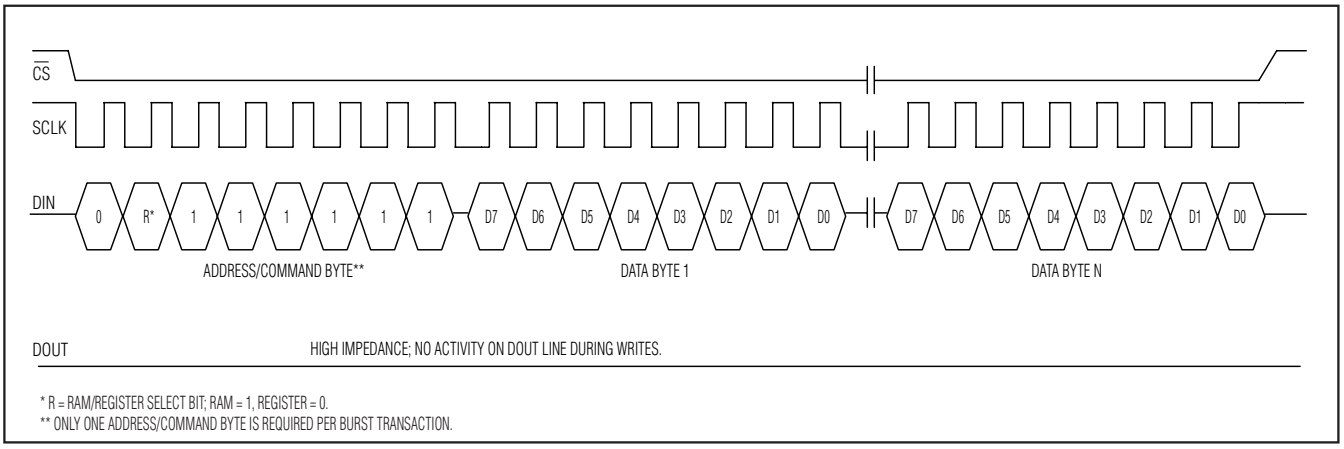


Figure 3b. Burst Write

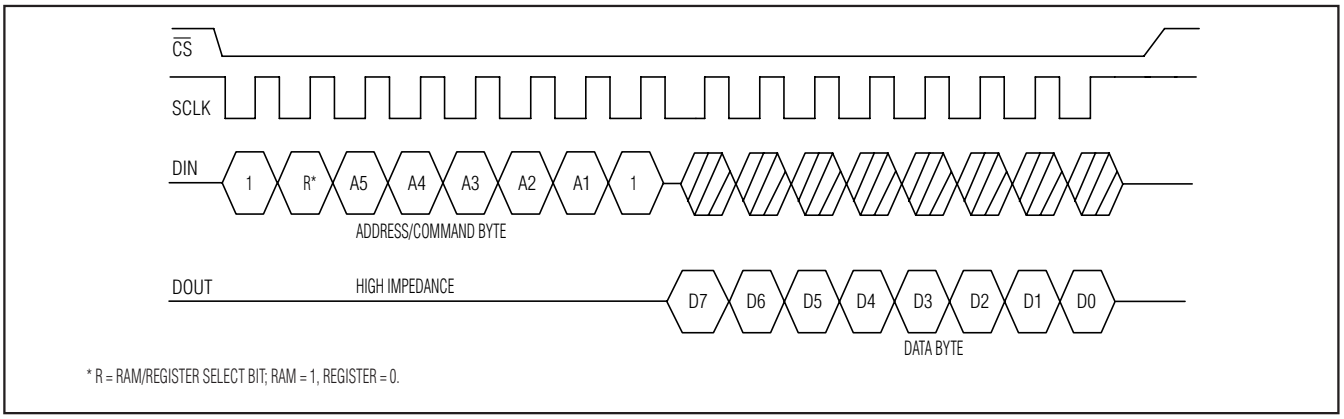


Figure 4a. Single Read

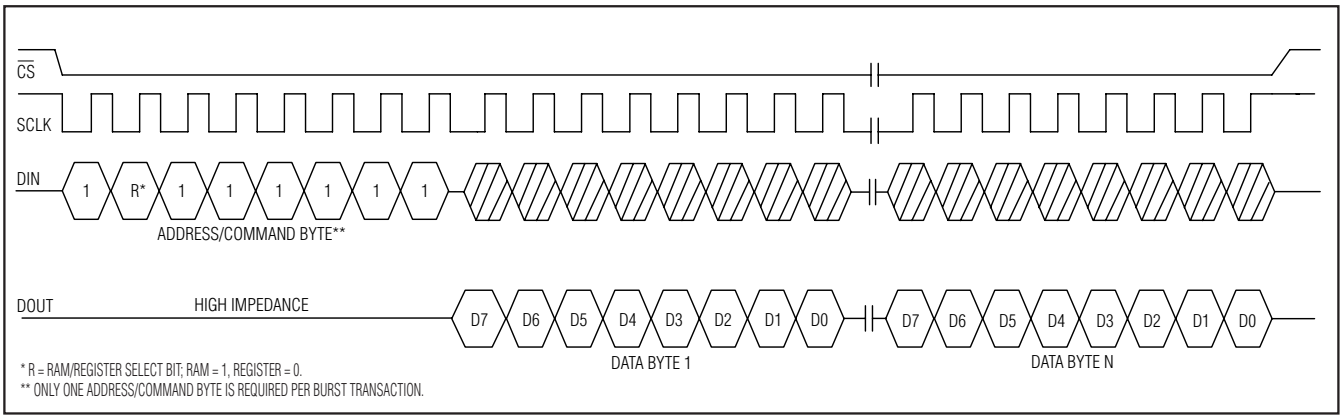


Figure 4b. Burst Read

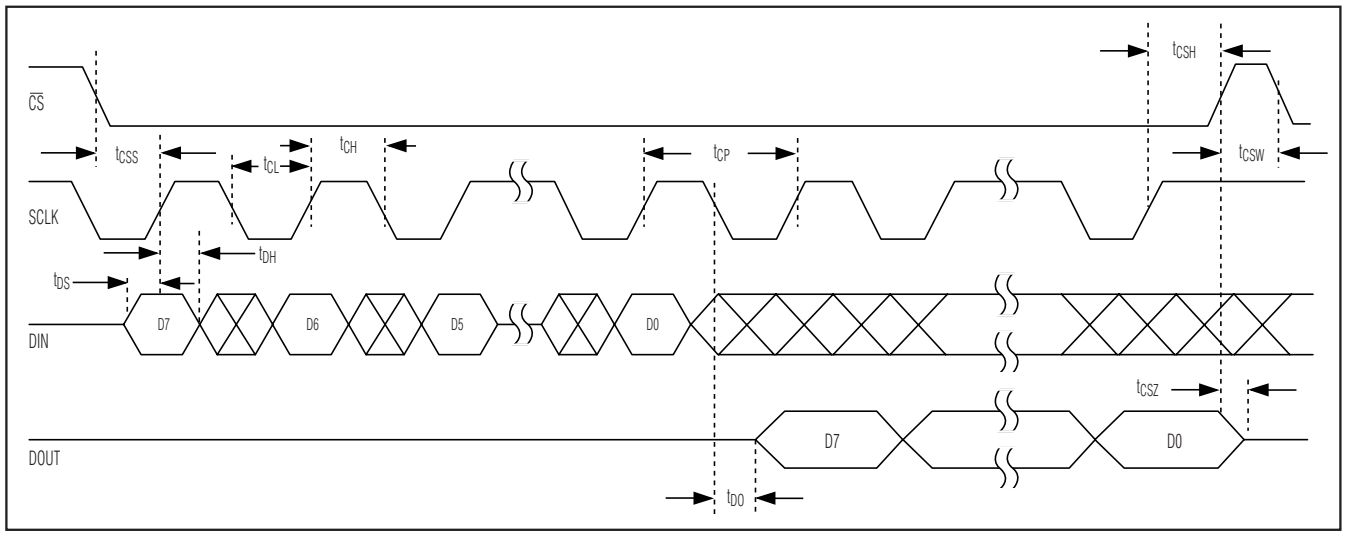


Figure 5. SPI Bus Timing Diagrams

Chip Select

$\overline{CS}$ serves two functions. First, $\overline{CS}$ turns on the control logic that allows access to the Shift register for Address/Command and data transfer. Second, $\overline{CS}$ provides a method of terminating either single-byte or multiple-byte data transfers. All data transfers are initiated by driving $\overline{CS}$ low. If $\overline{CS}$ is high, then DOUT is high impedance.

Serial Clock

A clock cycle on SCLK is a rising edge followed by a falling edge. For data input, data must be valid at DIN before the rising edge of the clock. For data outputs, bits are valid on DOUT after the falling edge of the clock.

Data Input (Single-Byte Write)

Following the eight SCLK cycles that input a Single-Byte Write Address/Command, data bits are input on the rising edges of the next eight SCLK cycles. Additional SCLK cycles are ignored. Input data MSB first.

Data Input (Burst Write)

Following the eight SCLK cycles that input a Burst-Write Address/Command, data bits are input on the rising edges of the following SCLK cycles. The number of clock cycles depends on whether the timekeeping registers or RAM are being written. A Clock Burst Write requires 1 Address/Command byte, 7 timekeeping data bytes, and 1 Control register byte. A Burst Write to RAM may be terminated after any complete data byte by driving $\overline{CS}$ high. Input data MSB first (Figure 3).

Data Output (Single-Byte Read and Burst Read)

A read from the MAX6902 is initiated by an Address/Command Write from the microcontroller (master) to the MAX6902 (slave). The Address/Command Write portion of the data transfer is clocked into the MAX6902 on rising clock edges. Following the eighth falling clock edge of SCLK, after t_{DO} (Figure 4) data begins to be output on DOUT of the MAX6902. Data bytes are output MSB first. Additional SCLK cycles transmit additional data bits, as long as $\overline{CS}$ remains low. This permits continuous burst-mode read capability.

Applications Information

Crystal Selection

The MAX6902 is designed to use a standard 32.768kHz watch crystal. Table 1 details the recommended crystal requirements. Some suggested crystals are listed in Table 3. In addition to the specified SMT devices, some of the listed manufacturers also offer other package options.

Frequency Stability and Temperature

Timekeeping accuracy of the MAX6902 is dependent on the frequency stability, of the external crystal. To determine frequency stability, use the parabolic curve in Figure 6 and the following equations:

$$\Delta f = fk(T_0 - T)^2$$

where:

Δf = change in frequency from +25°C (Hz)

f = nominal crystal frequency (Hz)

SPI-Compatible RTC in a TDFN

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)