19-2085; Rev 2; 5/04

3-Wire Serial RTC in a TDFN

General Description

The MAX6901 3-wire serial interface real-time clock in a TDFN package contains a real-time clock/calendar and 31 x 8 bits of static RAM (SRAM). The real-time clock/calendar provides seconds, minutes, hours, day, date, month, year, and century information. A time/date-programmable polled ALARM is included in the MAX6901. The end of the month date is automatically adjusted for months with fewer than 31 days, including corrections for leap year up to the year 2100. The clock operates in either the 24hr or 12hr format with an AM/PM indicator. A push-pull 32kHz output is also included. The MAX6901 operates with a supply voltage of +2V to +5.5V, is available in the ultra-small 8-pin TDFN package, and works over the industrial temperature range, -40°C to +85°C.

Applications

Point-of-Sale Equipment

Intelligent Instruments

Fax Machines

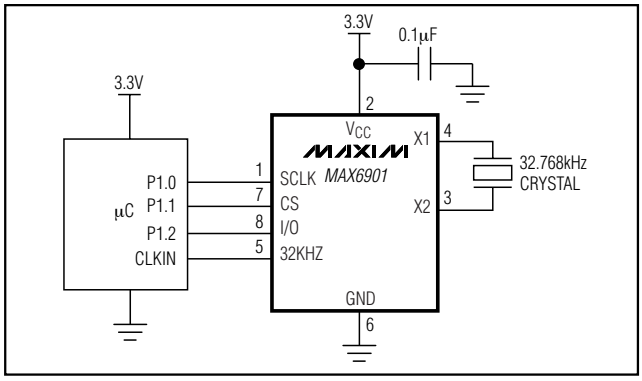
Battery-Powered Products

Portable Instruments

Features

- **Real-Time Clock Counts Seconds, Minutes, Hours, Day of Week, Date of Month, Month, Year, and Century**
- **Leap-Year Compensation Valid up to Year 2100**
- **Wide +2V to +5.5V Operating Voltage Range**
- **3-Wire Serial Interface, 2MHz at 5V, 500kHz at 2V**
- **31 x 8-Bit SRAM for Scratchpad Data Storage**
- **Uses Standard 32.768kHz, 12.5pF Watch Crystal**
- **Low Timekeeping Current (400nA at 2V)**
- **Single-Byte or Multiple-Byte (Burst Mode) Data Transfer for Read or Write of Clock Registers or SRAM**
- **8-Pin 3mm x 3mm x 0.8mm TDFN Surface-Mount Package**
- **Push-Pull 32.768kHz Clock Output**
- **Programmable Time/Date Polled ALARM Function**
- **No External Crystal Bias Resistors or Capacitors Required**

Typical Operating Circuit



Ordering Information

PART	TEMP RANGE	PIN-PACKAGE	TOP MARK
MAX6901ETA-T	-40°C to +85°C	8 TDFN	AGV

Pin Configuration appears at end of data sheet.

Functional Diagram appears at end of data sheet.

Related Real-Time Clock Products

PART	SERIAL INTERFACE	ALARM (bits)	ALARM FUNCTION	OUTPUT FREQUENCY	PIN-PACKAGE
MAX6900	I^2C compatible	31 x 8	—	—	6 TDFN
MAX6901	3 wire	31 x 8	Polled	32kHz	8 TDFN
MAX6902	SPI™ compatible	31 x 8	Polled	—	8 TDFN

SPI is a trademark of Motorola, Inc.

3-Wire Serial RTC in a TDFN

Table 2. Register Address/Definition

FUNCTION	REGISTER ADDRESS A7	A6	A5	A4	A3	A2	A1	A0		REGISTER DEFINITION VALUE	D7	D6	D5	D4	D3	D2	D1	D0
TIMEKEEPING																		
SECOND	1	0	0	0	0	0	0	RD /W		00-59	32kHz EN	10 SEC			1 SEC			
										*POR STATE	0	0	0	0	0	0	0	0
MINUTE	1	0	0	0	0	0	1	RD /W		00-59	ALM OUT	10 MIN			1 MIN			
										*POR STATE	0	0	0	0	0	0	0	0
HOUR	1	0	0	0	0	1	0	RD /W		00-23	12/24	0	10 HR	10 HR	1 HR			
										01-12	1/0		A/P 0/1					
										*POR STATE	0	0	0	0	0	0	0	0
DATE	1	0	0	0	0	1	1	RD /W		01-28/29 01-30 01-31	0	0	10 DATE		1 DATE			
										*POR STATE	0	0	0	0	0	0	0	1
MONTH	1	0	0	0	1	0	0	RD /W		01-12	0	0	0	10M	1 MONTH			
										*POR STATE	0	0	0	0	0	0	0	1
DAY	1	0	0	0	1	0	1	RD /W		01-07	0	0	0	0	0	WEEKDAY		
										*POR STATE	0	0	0	0	0	0	0	1
YEAR	1	0	0	0	1	1	0	RD /W		00-99	10 YEAR				1 YEAR			
										*POR STATE	0	1	1	1	0	0	0	0
CONTROL	1	0	0	0	1	1	1	RD /W			WP	0	0	0	0	0	0	0
										*POR STATE	0	0	0	0	0	0	0	0
CENTURY	1	0	0	1	0	0	1	RD /W		00-99	1000 YEAR				100 YEAR			
										*POR STATE	0	0	0	1	1	0	0	1

Note: *POR STATE defines power-on reset state of register content.

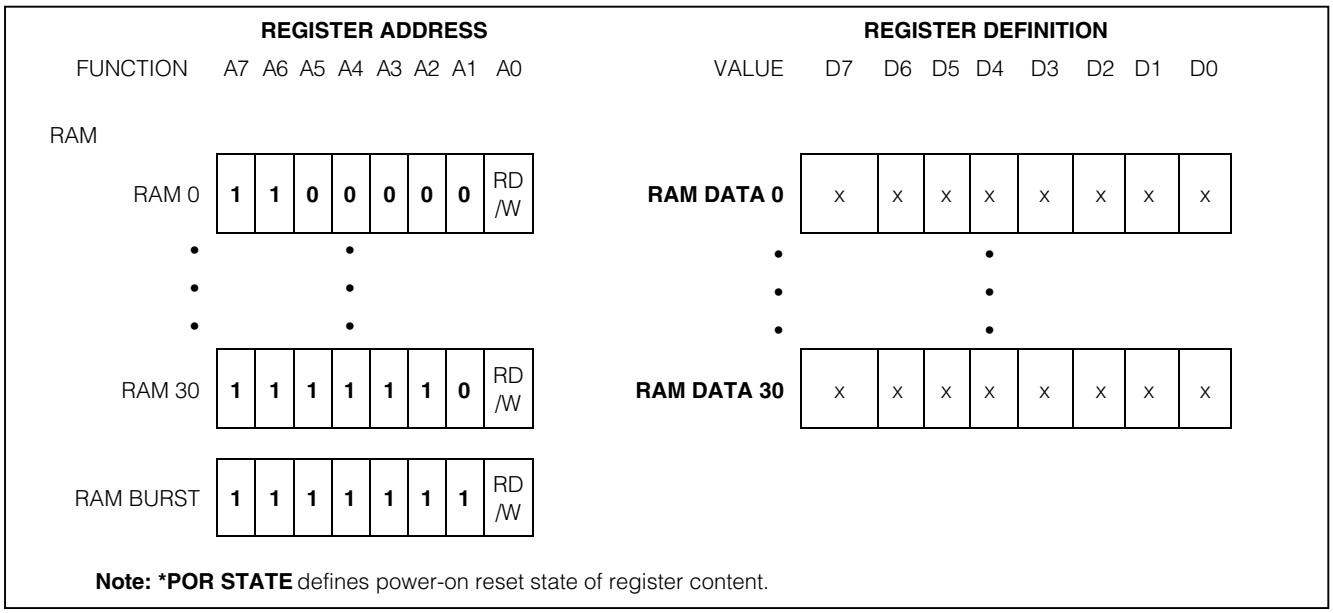
then read the Seconds register again (final-seconds). Check to see that final-seconds is equal to initial-seconds. If not, repeat the write process. If the Seconds register is to be written, update the Seconds register first, and then read it back and store its value (initial-seconds). Update the remaining timekeeping registers and then read the Seconds register again (final-sec-

Table 2. Register Address/Definition (continued)

FUNCTION	REGISTER ADDRESS A7	A6	A5	A4	A3	A2	A1	A0	REGISTER DEFINITION VALUE	D7	D6	D5	D4	D3	D2	D1	D0
ALARM CONFIG	**1**	**0**	**0**	**1**	**0**	**1**	**0**	RD /W		0	YEAR	DAY	MONTH	DATE	HOUR	MINUTE	SECOND
									***POR STATE**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
RESERVED Do not write to this location.	1	0	0	1	0	1	1	RD /W		0	0	0	0	0	1	1	1
									***POR STATE**	0	0	0	0	0	1	1	1
ALARM THRESHOLDS																	
SECOND	**1**	**0**	**0**	**1**	**1**	**0**	**0**	RD /W	00-59	0	10 SEC			1 SEC			
									***POR STATE**	**0**	**1**	**1**	**1**	**1**	**1**	**1**	**1**
MINUTE	**1**	**0**	**0**	**1**	**1**	**0**	**1**	RD /W	00-59	0	10 MIN			1 MIN			
									***POR STATE**	**0**	**1**	**1**	**1**	**1**	**1**	**1**	**1**
HOUR	**1**	**0**	**0**	**1**	**1**	**1**	**0**	RD /W	00-23	12/24	0	10 HR	10 HR	1 HR			
									01-12	1/0		A/P 0/1					
									***POR STATE**	**1**	**0**	**1**	**1**	**1**	**1**	**1**	**1**
DATE	**1**	**0**	**0**	**1**	**1**	**1**	**1**	RD /W	01-28/29 01-30 01-31	0	0	10 DATE		1 DATE			
									***POR STATE**	**0**	**0**	**1**	**1**	**1**	**1**	**1**	**1**
MONTH	**1**	**0**	**1**	**0**	**0**	**0**	**0**	RD /W	01-12	0	0	0	10 M	1 MONTH			
									***POR STATE**	**0**	**0**	**0**	**1**	**1**	**1**	**1**	**1**
DAY	**1**	**0**	**1**	**0**	**0**	**0**	**1**	RD /W	01-07	0	0	0	0	0	WEEKDAY		
									***POR STATE**	**0**	**0**	**0**	**0**	**0**	**1**	**1**	**1**
YEAR	**1**	**0**	**1**	**0**	**0**	**1**	**0**	RD /W	00-99	10 YEAR				1 YEAR			
									***POR STATE**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**
CLOCK BURST	**1**	**0**	**1**	**1**	**1**	**1**	**1**	RD /W									

Note: *POR STATE defines power-on reset state of register content.

Table 2. Register Address/Definition (continued)



Note: *POR STATE defines power-on reset state of register content.

onds). Check to see that final-seconds is equal to initial-seconds. If not, repeat the write process.

Note: After writing to any time or date register, no read or write operations are allowed for 45µs.

AM/PM and 12Hr/24Hr Mode

Bit 7 of the Hours register selects 12hr or 24hr mode. When high, 12hr mode is selected. In 12hr mode, bit 5 is the AM/PM bit, logic high for PM. In 24hr mode, bit 5 is the second 10hr bit, logic high for hours 20 through 23.

Write-Protect Bit

Bit 7 of the Control register is the write-protect bit. When high, the write-protect bit prevents write operations to all registers except itself. After initial settings are written to the timekeeping registers, set the write-protect bit to logic 1 to prevent erroneous data from entering the registers during power glitches or interrupted serial transfers. The lower 7 bits (bits 0–6) are unusable, and always read zero. Any data written to bits 0–6 are ignored. Bit 7 must be set to zero before a single byte write to the clock, before a write to RAM, or during a burst write to the clock.

Example: Setting the Clock with a Burst Write

To set the clock with a Burst Write operation to 10:11:31PM, Thursday July 4th, 2002, write BEh as Address/Command byte, followed by 8 bytes, B1h, 11h, B0h, 04h, 07h, 04h, 02h, and 00h (Table 2). BEh accesses the Clock Burst Write register. The first byte, B1h, sets the Seconds register to 31, and disables the 32.768kHz output. The second byte, 11h, sets the Minutes register to 11. The third byte, B0h, sets the Hours register to 12hr mode, and 10PM. The fourth byte, 04h, sets the Date register (day of the month) to the 4th. The fifth byte, 07h, sets the Month register to July. The sixth byte, 04h, sets the Day register (day of the week) to Thursday. The seventh byte, 02h, sets the Year register to 02. The eighth byte, 00h, clears the write-protect bit of the Control register to allow writing to the MAX6901. The Century register is not accessed with a Burst Write and therefore must be written to separately to set the century to 20. Note the Century register corresponds to the thousand and hundred digits of the current year and defaults to 19.

Reading the Clock

Reading the Timekeeping Registers

The main timekeeping registers (Seconds, Minutes, Hours, Date, Month, Day, Year) can be read with either Single Reads or a Burst Read. In the MAX6901, a latch buffers each clock counter's data. Clock counter data are latched by the 3-wire serial Read command (on the falling edge of SCLK, after the Address/Command byte has been sent by the Master to read a timekeeping register). Collision-detection circuitry ensures that this

Table 3. HEX Register Address/Description

WRITE ADDRESS/COMMAND BYTE (HEX)	READ ADDRESS/COMMAND BYTE (HEX)	DESCRIPTION	POR CONTENTS (HEX)
80	81	SECONDS	00
82	83	MINUTES	00
84	85	HOUR	00
86	87	DATE	01
88	89	MONTH	01
8A	8B	DAY	01
8C	8D	YEAR	70
8E	8F	CONTROL	00
90	91	RESERVED	Nonapplicable
92	93	CENTURY	19
94	95	ALARM CONFIGURATION	00
96	97	RESERVED	07
98	99	SECONDS ALARM THRESHOLD	7F
9A	9B	MINUTES ALARM THRESHOLD	7F
9C	9D	HOURS ALARM THRESHOLD	BF
9E	9F	DATE ALARM THRESHOLD	3F
A0	A1	MONTH ALARM THRESHOLD	1F
A2	A3	DAY ALARM THRESHOLD	07
A4	A5	YEAR ALARM THRESHOLD	FF
BE	BF	CLOCK BURST	Nonapplicable
C0	C1	RAM 0	Indeterminate
C2	C3	RAM 1	Indeterminate
C4	C5	RAM 2	Indeterminate
C6	C7	RAM 3	Indeterminate
C8	C9	RAM 4	Indeterminate
CA	CB	RAM 5	Indeterminate
CC	CD	RAM 6	Indeterminate
CE	CF	RAM 7	Indeterminate
D0	D1	RAM 8	Indeterminate
D2	D3	RAM 9	Indeterminate
D4	D5	RAM 10	Indeterminate
D6	D7	RAM 11	Indeterminate
D8	D9	RAM 12	Indeterminate
DA	DB	RAM 13	Indeterminate
DC	DD	RAM 14	Indeterminate
DE	DF	RAM 15	Indeterminate
E0	E1	RAM 16	Indeterminate
E2	E3	RAM 17	Indeterminate

Table 3. HEX Register Address/Description (continued)

WRITE ADDRESS/COMMAND BYTE (HEX)	READ ADDRESS/COMMAND BYTE (HEX)	DESCRIPTION	POR CONTENTS (HEX)
E4	E5	RAM 18	Indeterminate
E6	E7	RAM 19	Indeterminate
E8	E9	RAM 20	Indeterminate
EA	EB	RAM 21	Indeterminate
EC	ED	RAM 22	Indeterminate
EE	EF	RAM 23	Indeterminate
F0	F1	RAM 24	Indeterminate
F2	F3	RAM 25	Indeterminate
F4	F5	RAM 26	Indeterminate
F6	F7	RAM 27	Indeterminate
F8	F9	RAM 28	Indeterminate
FA	FB	RAM 29	Indeterminate
FC	FD	RAM 30	Indeterminate
FE	FF	RAM Burst	Nonapplicable

does not happen coincident with a Seconds counter increment to ensure accurate time data is being read. The clock counters continue to count and keep accurate time during the Read operation.

The simplest way to read the timekeeping registers is to use a Burst Read. In a Burst Read, the main timekeeping registers (Seconds, Minutes, Hours, Date, Month, Day, Year) and the Control register are read sequentially in the order listed with the Seconds register first. They are read out as a group of eight registers, with 8 bits each. All timekeeping registers (except Century) are latched upon the receipt of the Burst Read command. The worst-case error between the "actual" time and the "read" time is 1 second for a normal data transfer.

The timekeeping registers may also be read using Single Reads. If Single Reads are used, it is necessary to do some error checking on the receiving end, because it is possible that the clock counters could change during the Read operations, and report inaccurate time data. The potential for error is when the Seconds register increments before all the registers are read. For example, suppose a carry of 13:59:59 to 14:00:00 occurs during Single Read operations. The net data read could be 14:59:59, which is erroneous. To prevent errors from occurring with Single Read operations, read the Seconds register first (initial-seconds) and store this value for future comparison. After the remaining timekeeping registers have been read, reread the Seconds register (final-seconds). Check that the final-seconds value equals the initial-seconds value; if not, repeat the entire Single Read process. Using Single Reads at a 100kHz serial speed, it takes under 2.5ms to read all seven of the timekeeping registers, including two reads of the Seconds register.

Example: Reading the Clock with a Burst Read

To read the time with a Burst Read, send BFh as the Address/Command byte. Then clock out 8 bytes, Seconds, Minutes, Hours, Date of the month, Month, Day of the week, Year, and finally the Control byte. All data are output LSB first. Decode the required information based on the register definitions listed in Table 2.

Using the Alarm

A polled alarm function is available by reading the ALM OUT bit. The ALM OUT bit is D7 of the Minutes timekeeping register. A logic 1 in ALM OUT indicates the alarm function is triggered. There are eight registers associated with the alarm function, seven programmable Alarm Threshold registers and one programmable Alarm Configuration register. The Alarm Configuration register determines which Alarm Threshold registers are compared to the timekeeping registers, and the ALM OUT bit sets if the compared registers are equal. Table 2 shows the function of each bit of the Alarm Configuration register. Placing a logic 1 in any given bit of the Alarm Configuration register enables the respec-

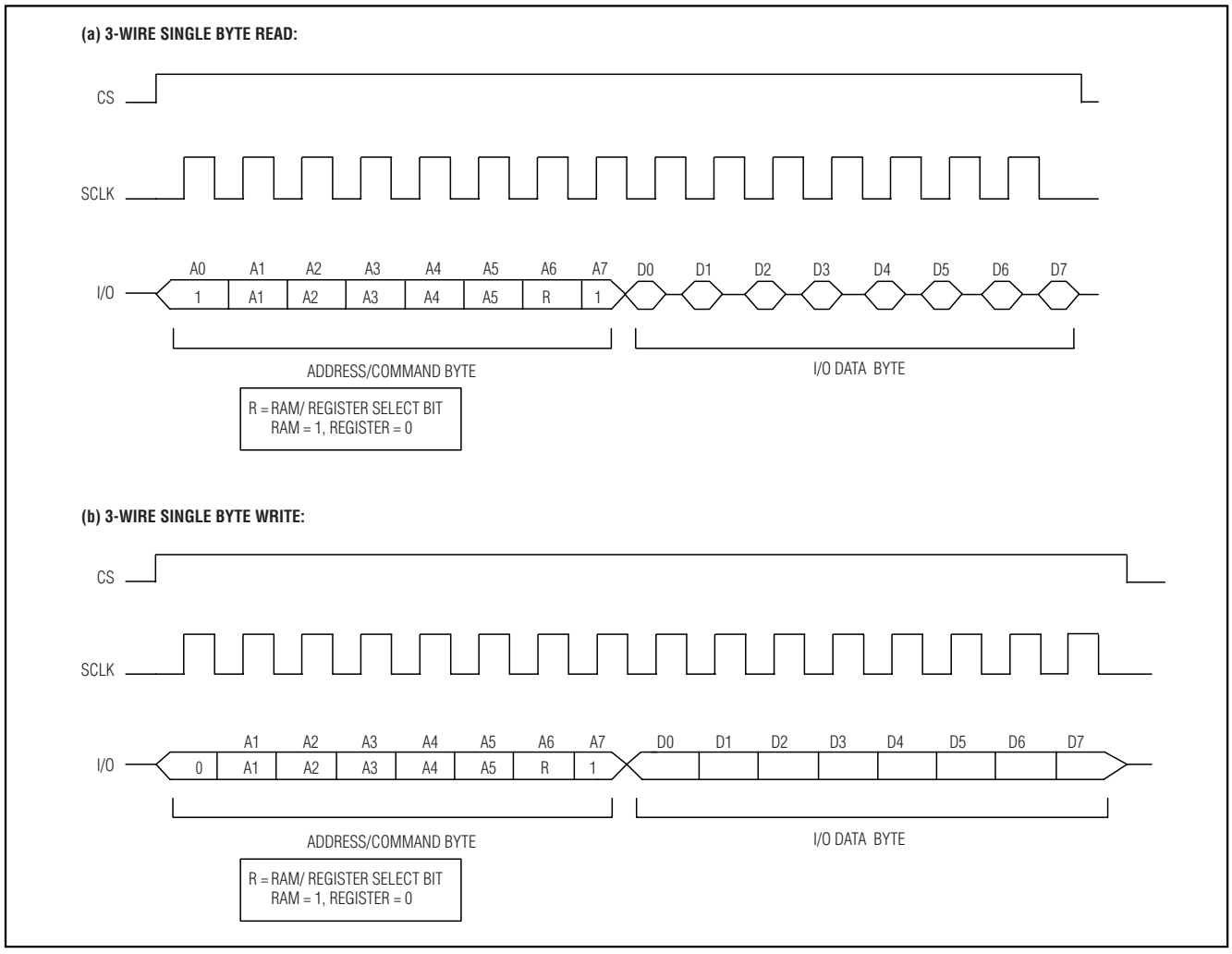


Figure 2. Single Byte Data Transfer

32.768kHz Output (32KHZ)

32KHZ is a push-pull 32.768kHz output for timing or clocking of external devices. Bit D7 in the Clock Seconds register is the active-low enable bit for 32KHZ. When D7 is logic 0, 32KHZ is enabled. When logic 1, 32KHZ is disabled and set to high impedance. Power-on reset enables the 32.768kHz output.

Applications Information

Crystal Selection

The MAX6901 is designed to use a standard 32.768kHz watch crystal. Table 1 details the recommended crystal requirements. Some suggested crystals are listed in Table 4. In addition to the specified SMT devices, some of the listed manufacturers also offer other package options.

Frequency Stability and Temperature

Timekeeping accuracy of the MAX6901 is dependent on the frequency stability of the external crystal. To determine frequency stability, use the parabolic curve in Figure 6 and the following equations:

$$\Delta f = fk (T_0 - T)^2$$

where:

Δf = change in frequency from +25°C

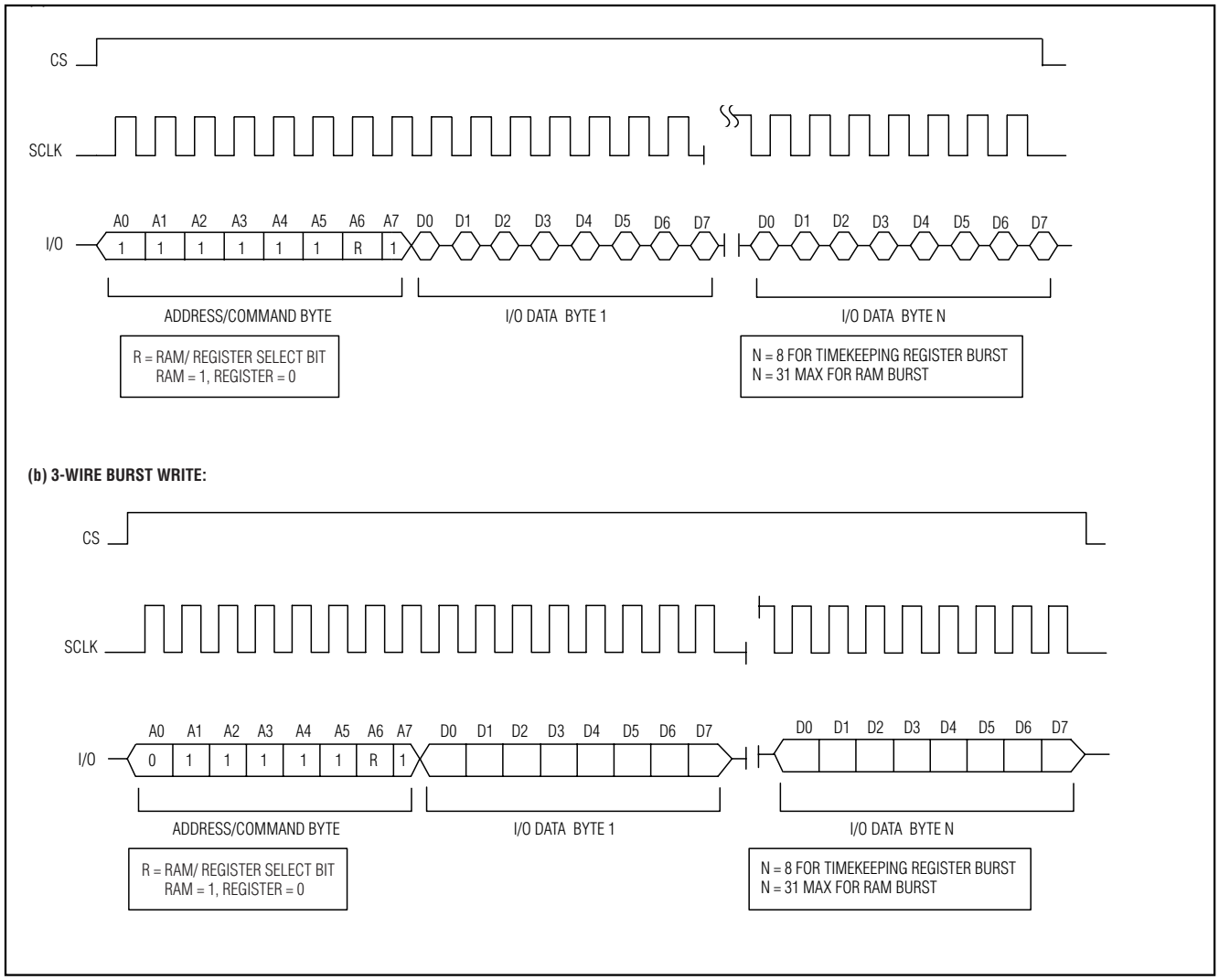


Figure 3. Burst Mode Data Transfer

f = nominal crystal frequency

k = parabolic curvature constant (-0.035ppm/°C2 ±0.005ppm/°C2 for 32.768kHz watch crystals)

T_0 = turnover temperature (+25°C ±5°C for 32.768kHz watch crystals)

T = temperature of interest (°C)

For example: What is the worst-case change in oscillator frequency from +25°C ambient to +45°C ambient?

$$\Delta f_{drift} = 32{,}768 \times (-0.04 \times (1 \times 10^{-6})) \times (20-45)^2$$
$$= -0.8192Hz$$

What is the worst-case timekeeping error per second?

Error due to temperature drift:

$$\Delta t_{drift} = \{[1 / [(f+\Delta f_{drift}) / 32768]]-1s\} / 1s$$

$$\Delta t_{drift} = \{[1 / [(32768 - 0.8192) / 32768]]-1\}/1s$$
$$= 0.000025s/s$$

Error due to +25°C initial crystal tolerance of ±20ppm:

$$\Delta f_{initial} = 32{,}768 \times (-20 \times ((1 \times 10\text{-}6)) = -0.65536Hz$$

$$\Delta t_{initial} = \{[1 / [(f+\Delta f_{initial}) / 32768]]-1s\} / 1s$$

$$\Delta t_{initial} = \{[1 / [(32768-0.65536) / 32768]]-1\} / 1s$$
$$= 0.000025s/s$$

Total timekeeping error per second:

3-Wire Serial RTC in a TDFN

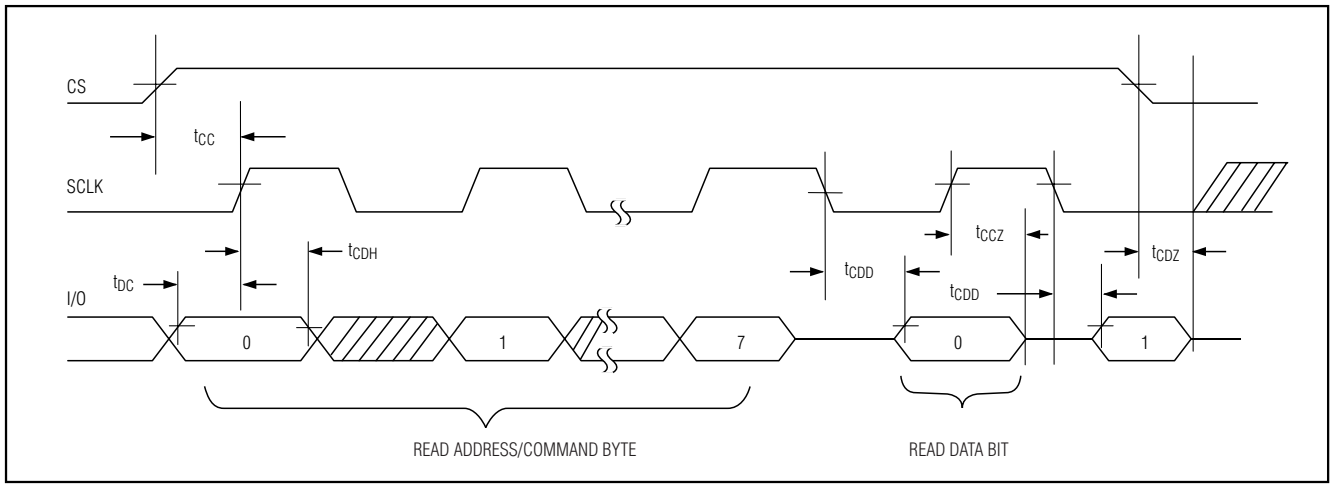


Figure 4. 3-Wire Read Data Transfer Serial Timing Diagram

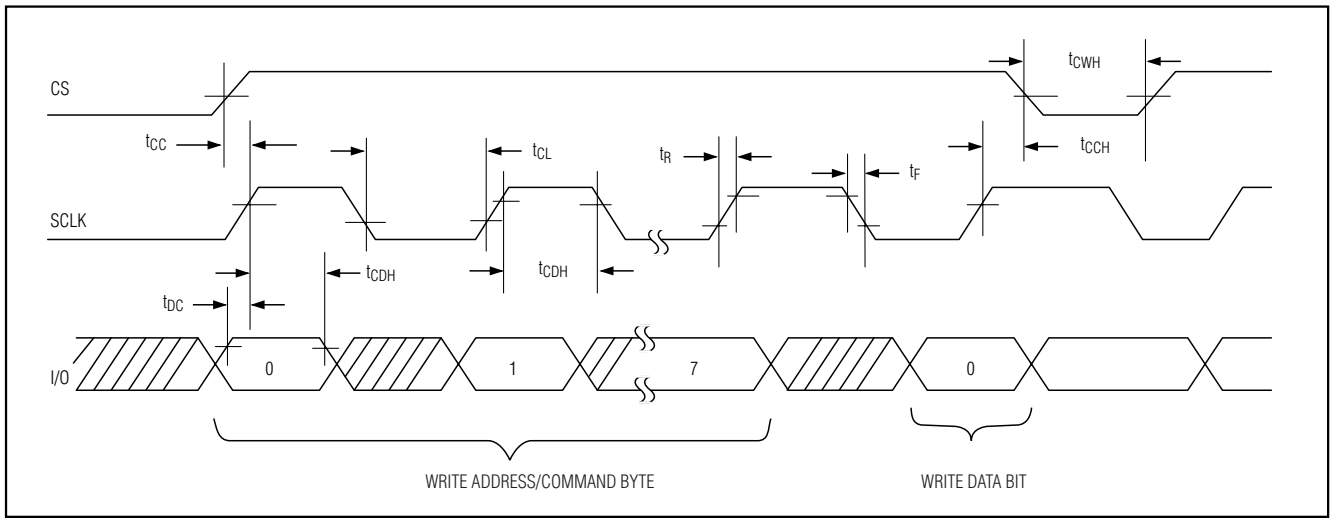


Figure 5. 3-Wire Write Data Transfer Serial Timing Diagram

$$\Delta t_{total} = \Delta t_{drift} + \Delta t_{initial}$$

$$\Delta t_{total} = 0.00002+0.000025=0.000045s/s$$

$$\Delta t = \left(31\,days\right)\times\left(24\frac{hr}{day}\right)\times\left(60\frac{min}{hr}\right)\times\left(60\frac{s}{min}\right)\times$$

$$\left(0.00045s/s\right)=120.528s$$

Total worst-case timekeeping error at the end of 1 month at +45°C is about 120s or 2 min (assumes negligible parasitic layout capacitance).

Oscillator Start Time

The MAX6901 oscillator typically takes 5s to 10s to begin oscillating. To ensure the oscillator is operating correctly, the software should validate proper timekeeping. This is accomplished by reading the Seconds register. Any reading of 1s or more from the POR value of zero is a validation of proper startup.

Power-On Reset

The MAX6901 contains an integral POR circuit that ensures all registers are reset to a known state on power-up. Once V_{CC} rises above 1.6V (typ), the POR circuit releases the registers for normal operation. When

3-Wire Serial RTC in a TDFN

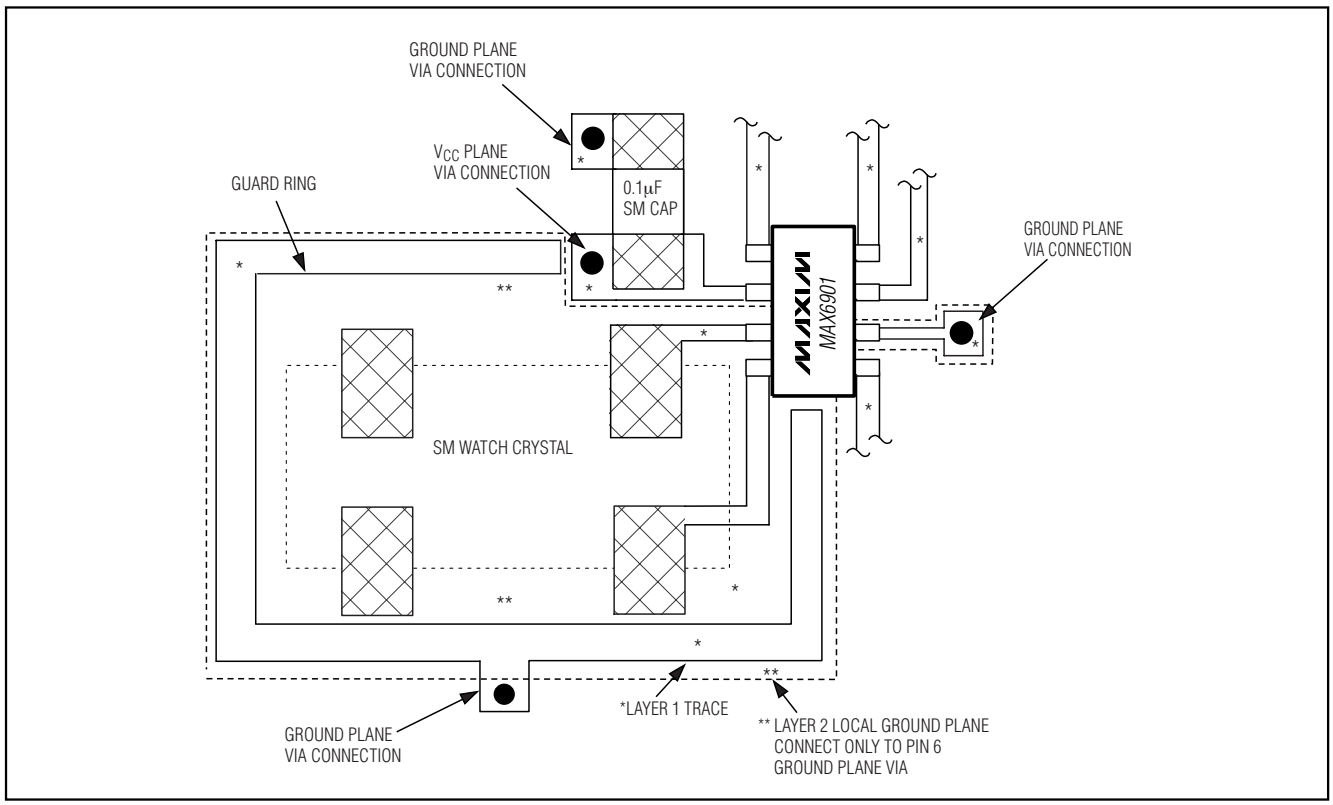


Figure 7. Printed Circuit Board Layout for Crystal Connections

There are similar considerations for 32KHZ if it is placed in its high-impedance state. For lowest timekeeping current, it should not be allowed to float. Force it high or low, or terminate it with a pullup or pulldown resistor.

PC Board Layout Considerations

The MAX6901 uses a very-low-current oscillator to minimize supply current. This causes the oscillator pins, X1 and X2, to be relatively high impedance. Exercise care to prevent unwanted noise pickup.

Connect the 32.768kHz crystal directly across X1 and X2 of the MAX6901. To eliminate unwanted noise pickup, design the PC board using these guidelines (Figure 7): place the crystal as close to X1 and X2 as possible and keep the trace lengths short; place a guard ring around the crystal, X1 and X2 traces (where applicable), and connect the guard ring to GND; keep all signal traces away from beneath the crystal, X1, and X2. Finally, an additional local ground plane can be added under the crystal on an adjacent PC board layer. The plane should be isolated from the regular PC board ground plane, and tied to ground at the MAX6901 ground pin. Restrict the plane to be no larger than the perimeter of the guard ring. Do not allow this ground plane to contribute significant capacitance between X1 and X2.

Chip Information

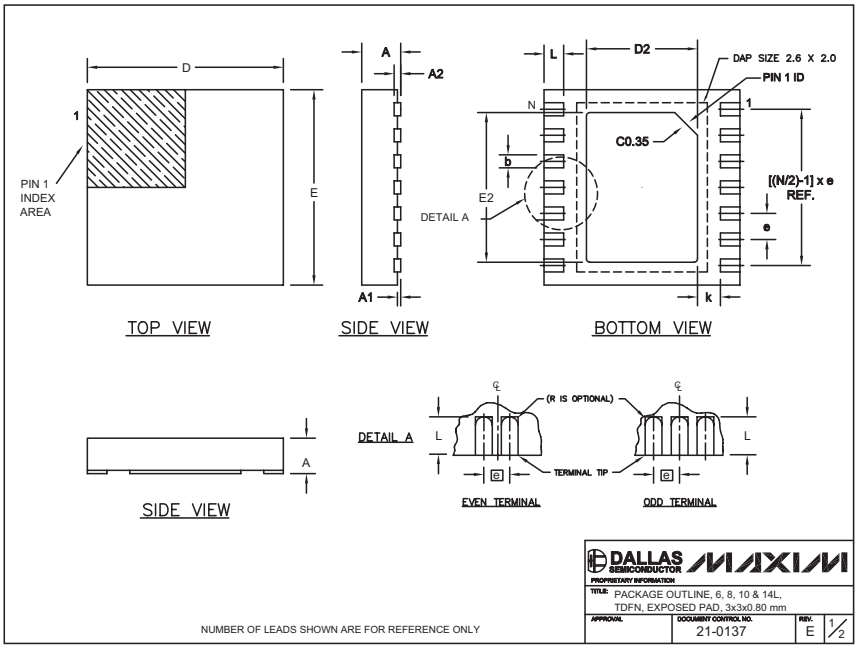
TRANSISTOR COUNT: 26,214

PROCESS: CMOS

3-Wire Serial RTC in a TDFN

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline info rmation go to **www.maxim-ic.com/packages**.)



COMMON DIMENSIONS		
SYMBOL	MIN.	MAX.
A	0.70	0.80
D	2.90	3.10
E	2.90	3.10
A1	0.00	0.05
L	0.20	0.40
k	0.25 MIN.	
A2	0.20 REF.	

PACKAGE VARIATIONS							
PKG. CODE	N	D2	E2	e	JEDEC SPEC	b	[(N/2)-1] x e
T633-1	6	1.50±0.10	2.30±0.10	0.95 BSC	MO229 / WEEA	0.40±0.05	1.90 REF
T833-1	8	1.50±0.10	2.30±0.10	0.65 BSC	MO229 / WEEC	0.30±0.05	1.95 REF
T1033-1	10	1.50±0.10	2.30±0.10	0.50 BSC	MO229 / WEED-3	0.25±0.05	2.00 REF
T1433-1	14	1.70±0.10	2.30±0.10	0.40 BSC	- - - -	0.20±0.03	2.40 REF

NOTES:
1. ALL DIMENSIONS ARE IN mm. ANGLES IN DEGREES.
2. COPLANARITY SHALL NOT EXCEED 0.08 mm.
3. WARPAGE SHALL NOT EXCEED 0.10 mm.
4. PACKAGE LENGTH/PACKAGE WIDTH ARE CONSIDERED AS SPECIAL CHARACTERISTIC(S).
5. DRAWING CONFORMS TO JEDEC MO229, EXCEPT DIMENSIONS "D2" AND "E2", AND T1433-1.
6. "N" IS THE TOTAL NUMBER OF LEADS.

DALLAS SEMICONDUCTOR MAXIM
PROPRIETARY INFORMATION
TITLE: PACKAGE OUTLINE, 6, 8, 10 & 14L, TDFN, EXPOSED PAD, 3x3x0.80 mm
APPROVAL
DOCUMENT CONTROL NO. 21-0137
REV. E
2/2