Master of Engineering in VLSI Systems
**Course Structure:**

The new course will be offered in two modes, part-time and full-time.

The part-time mode is designed to facilitate students currently in employment. It is a block-release course (with lectures offered on a single day per week during the academic term). It requires attendance at lectures over four academic terms, spanning two years.

In full-time mode the course spans a single academic year, and requires full-time student attendance on campus.

The part-time and the full-time version of the course have the same academic content.

The course consists of a taught component and a project. The taught material comprises ten modules, each of which is worth three credits. The project comprises two nine-credit modules. Hence, the total credit weighting of the course is 48 credits, 30 of which (62.5% of the total weighting) are taught material, and 18 (37.5%) project-based.

For students on the part-time version of the course there will be a maximum completion time allowed of four years. Any student who does not complete both the taught and the project components of the part-time course in a satisfactory fashion within this period will not be awarded a M.Eng. in VLSI Systems. If the student has completed the taught component only, but not the project component, he/she may be awarded a Graduate Diploma in VLSI Systems.

There is, similarly, a maximum completion time allowed for students on the full-time version of the course. In this case it is two years. A student who completes the taught component of the course within two years, but not the project component, may be awarded a Graduate Diploma in VLSI Systems.

Students on the part-time version of the course will study three modules per semester in the first academic year of their programme. In the second academic year, they will study two modules per semester and undertake the project work in parallel with this.

Students on the full-time version of the course will study five modules per semester and will also undertake project work in parallel.
### Part-Time Mode, Year 1

<table>
<thead>
<tr>
<th>Autumn Semester</th>
<th>Spring Semester</th>
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<tbody>
<tr>
<td>ASICS 1 (Digital)</td>
<td>ASICS 2 (Analogue)</td>
</tr>
<tr>
<td>Test Engineering 1</td>
<td>Test Engineering 2</td>
</tr>
<tr>
<td>Semiconductor Technology</td>
<td>Noise</td>
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</tbody>
</table>

### Part-Time Mode, Year 2

<table>
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<tr>
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<th>Spring Semester</th>
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<tbody>
<tr>
<td>Language Processors</td>
<td>Processor Architecture</td>
</tr>
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<td>Digital Control</td>
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<tr>
<td>Information Theory and Coding</td>
<td>Digital Communications</td>
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<tr>
<td>Advanced Digital System Design</td>
<td>Advanced Topic Seminars</td>
</tr>
<tr>
<td>Project 1 (9 credits)</td>
<td>Project 2 (9 credits)</td>
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*In year two of the part-time mode of this course the student may select any two of the four modules on offer per term.*

### Full-Time Mode

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*In full-time mode the student must study three core modules per term, and may select any two others from the four electives.*

- The course structure presented here is the result of significant consultation with industry (in particular, Analog Devices, Intel and Tellabs). Hence, it is designed to address skill shortages in the VLSI field.

- An innovative aspect of the course is the provision of a module, "Advanced Topic Seminars". This is designed to allow seminars to be presented by industry on specialist topics of interest to students. The idea is to enhance the flexibility of the course by allowing specialist material of current interest to be introduced easily and quickly. It is envisioned that the "Advanced Topic Seminars" module may vary in content from year to year and that it may be taught using "sandwich" techniques in the weeks prior to the start of the normal academic terms. As it may not be possible to provide a suitable "Advanced Topic Seminars" module every year, the course is designed so that they can run without it if necessary.
ASICS 1 (Digital ASICS)

This module introduces issues relating to the design and implementation of application-specific integrated circuits (ASICS) for digital systems.

Introduction to Design Methodology. Custom IC design. Standard cells. Programmable logic. Gate arrays. FPGAs. ASICs.
VLSI Structures. CMOS, advanced CMOS, ROMs and RAMs.
Design entry and simulation. Schematic capture. Simulation.
Device layout and fabrication. The CMOS IC fabrication process. The CMOS inverter. Other CMOS Structures (in an n-well process).

ASICS 2 (Analogue ASICS)

This module aims to provide an introduction to the design of full custom analogue ASICs (Application Specific Integrated Circuits).

Bipolar Junction Transistors and diodes. ESD protection structures. SPICE modelling of BJTs and diodes. Latch-up in circuits.
Analogue IC layout design. MOS transistors, capacitors, resistors, interconnect. CAD tool and design issues. CIF output.

Test Engineering 1 (Production Test Systems)

To provide the student with a good understanding of a complete product test system with particular emphasis on the role of modern programmable test systems (ATE).


Test Engineering 2 (Device and Circuit Level Test)

To provide a fundamental understanding of the principles, techniques and equipment for the testing of electronic products at the device and the system level in a production environment.

Relationship between reliability, maintainability and risk. Basic electronic system fault diagnosis. Fault diagnosis in circuits: analogue and digital. Component functional and parametric testing. VI
curve testing for 'black box' circuits. Test techniques for complex digital IC's, e.g. boundary scan. Signature analysis, test vectors, pseudo-random test patterns etc. BIST techniques. Role of diagnostic courses for self test. Review of some key test instruments.

**Semiconductor Technology**

This module introduces students to the fundamentals of VLSI manufacturing processes and technology.

**IC Technology:** Concept of die size and design rules; General overview of MOS and Bipolar technologies.

**Semiconductor Material:** Crystal growth, defects and processing of silicon; alloying; epitaxial growth.

**Deposition:** Atmospheric and low pressure chemical vapour deposition, polycrystalline and amorphous film deposition; evaporation; sputtering; properties of thin films: aluminium, refractory metals and silicides; Metalization; bonding; contacts; packaging.

**Oxidation:** Kinetics of thermal oxidation, dry, wet, pyrogenic, HCl and TCE ambient properties of interface, LOCOS.

**Diffusion:** P and N type impurities, Constant and limited source, annealing and diffusion in oxide; Gettering.

**Ion Implantation:** process technique, trajectories.

**Lithography:** Optical exposure and resist system, process characterization, mask making, wet and dry etching.

**Process Simulation:** lithography, oxidation, diffusion, etching.

**Process Integration:** Overview of Bipolar, NMOS, CMOS and BiCMOS technologies, threshold control, latch up prevention, parasitics; SOI and SOS technologies.

**Noise**

This module will equip the student with a sound understanding of the problems caused by noise in electrical networks. Both fundamental and man-made noise are discussed. Techniques to minimise noise are discussed.


Amplifier Noise: Representation of noise in amplifiers, equivalent input noise voltage and its equivalent input current and voltage sources. Noise Figure.

Semiconductor Noise: BJT noise model, noise in JFETS and MOSFETS.

Low Noise Amplifiers: Design.

Methods of noise and noise figure measurement.

Man Made Noise: European regulations, EMI emissions, EMI susceptibility, conducted and radiated noise.

Noise From PCBs: Track structures: strip line, microstrip and single sided board. Calculation of capacitive and inductive coupling between tracks as well as radiation from pcb tracks.

Power Line Noise: Noise on power supply lines and its minimisation. Power supply filters for minimisation of conducted noise, both common and differential mode.

Shielding: Effectiveness as function of frequency, shield thickness, conductivity and permeability. Effectiveness to inductive and radiated fields.

**Language Processors**

To introduce the theory of compiler design and show its application in a simple compiler. An important part of the module is the implementation of a compiler for a simple, Pascal-like, language.


**Parsing:** Top-down parsing. Lookahead. Recursive descent. LL(1) grammars. First, follow and predict sets.

**Syntactic error detection and recovery** for recursive descent parsers.

**Semantic processing:** The symbol table. Handling semantic errors.

**Code generation for a simple stack machine:** Translation of expressions to reverse-Polish form. Procedure calls and block structure. Static and dynamic scope. Storage management.

**Scanning:** Regular expressions. State machine implementation. Nondeterministic and deterministic automata. Scanner generators (LEX).

**Table-driven parsing techniques:** LL(1) table-driven parsers. Shift-reduce parsers. LR parsing. The LR(0) Characteristic Finite State Machine. LR(1). SLR. LALR(1). Parser generators (yacc).

**Processor Architecture**

To provide a grounding in the analytic study of computer architecture and an introduction to various architectural styles, e.g., CISC, RISC, and various non-von Neumann architectures.

**Review of Von-Neumann architecture:** Brief discussion of evolution in processor design from 1940's to today. Computer classifications. Flynn's taxonomy: SISD, SIMD, MIMD.

**Computer performance measurement:** Execution time and clock cycles per instruction (CPI). MIPS, MFLOPs. Benchmarks: Dhrystone, Whetstone. Kernels: Livermore loops, Linpack, SPECmarks.


**Instruction set design and architecture:** Classification. Register machines. Addressing modes. The role of high-level languages and compilers in determining instruction set architecture, "semantic gap", "high-level language architecture", CISC and RISC architectures.

**Processor implementation techniques:** Datapath. Execution steps. Control: hardwired, microcoded. Handling exceptions.


**Memory hierarchy design:** Register windows. Caches: strategies, replacement policies, block size. Main memory: width, interleaving. Virtual memory: page tables, translation lookaside buffers.

**Digital Signal Processing**

To introduce the theory of digital signal processing, including the following very important topics: the discrete Fourier Transform, the Z-transform and digital filter design.

Discrete signals & systems. The DFT, its properties and applications; relationship to other transforms; Fourier, Laplace, Z-transform etc. Railings as theoretical samplers. Spectral descriptions of sequences. Analogue and digital convolution, the z-transform in the design of FIR digital filters. Linear-phase, all-pass filters, & minimum-phase filters. Differentiators & Integrators. Windowing techniques in filter design. Filter design and fast convolution by FFT. Frequency-sampling filters. IIR filters: mapping from analogue filters, bi-linear mapping, review of other mappings, their application in digital and sampled-data (e.g. switched-capacitor) filters. Up-sampling and downsampling. band-pass signals & modulation. Finite word-length effects; impact on architectures. Noise topics. Sigma-delta noise shaping, applications in A/D and D/A conversion. Correlation principles. Fast correlation by DFT. Introduction to adaptive filtering. Wiener filter. LMS algorithm. Selected applications. Power spectra and spectral estimation.
Digital Control

To study the application of digital computers to control engineering problems.

Brief review of classical control system techniques covering stability analysis and design methods for both continuous and sampled data systems including Nyquist, Bode, root locus. Design criteria including gain and phase margin, settling and rise time, steady state and following error. Classical design techniques for, and implementation of, digital control systems; pole placement using state variable approach, direct design including deadbeat control, attenuation of ringing poles and multivariable design. Error mechanisms and sources including the algorithm, sampler, and word length. Issues having a significant impact on the practical implementation of digital controllers such as direct and canonical form for controller realisation, word length choice and processor hardware requirements. Development and testing; software structures; introduction to modern control techniques such as system identification, robust and optimal control.

Information Theory and Coding

This module aims to guide the student through the implications and consequences of fundamental theories and laws of information theory and to impart a comprehensive grounding in random and burst error protection coding theory with reference to their increasingly wide application in present day digital communications and computer systems.


MULTIPLE ACCESS, TDMA, FDMA and CDMA.
Carrier Recovery, Clock Recovery. Bit and frame synchronisation, phase lock loops, early-late gate.
ADAPTIVE EQUALISATION: Linear and Decision Feedback Equalisation, LMS and RLS.


Digital Communications

This module is intended to provide a comprehensive coverage of digital communication systems, the signals and key processing steps are traced from the information source through the transmitter, channel, receiver and ultimately to the information sink.

Communication Theory: Nyquist Criteria, Shannon Sampling Theorem, Intersymbol interference and Aliasing.
Digital Signal Processing for voice and data communication systems. Performance criteria, SNR and probability of error.
Properties of line codes (Bipolar, manchester coding, HDBn, 4B3T etc).
Multiple Access, TDMA, FDMA and CDMA.
The Channel: AWGN, Linear Time Invariant (LTI) and Time varying.
Synchronization: Carrier and clock recovery.
Adaptive Equalization.
Case study on a Spread Spectrum modem outlining the above principles is presented.

**Advanced Digital System Design**

This module aims to equip the student with a range of techniques applicable to the design and test of very high speed and fault-tolerant digital circuits.

**Review:** High-speed design in the time and frequency domains; reflection, ringing and crosstalk, transmission lines.

**Transmission lines and termination strategies:** Series, Thevenin, diode and AC terminations; Crosstalk, reflections, ground bounce. Properties and behaviour of stripline and microstrip traces.

**Technology review:** LVDS, ECL/PECL, GTL, SSTL, HSTL, and high-speed CMOS drivers and receivers; mixed voltage systems; bus-hold and bus-loading considerations; hot insertion.

**Synchronous Design:** Clock oscillators and buffering, Clock Distribution, Metastability.

**System Design and Manufacture:** PCB materials; Layer build and specification; Power supply considerations; Decoupling techniques.

**EMC/ESD:** Radiated vs conducted; Filtering; Effects of apertures, gasketing; Conducted emissions, co-axial cables, twisted pair; Shielding.

**Thermal Aspects:** Sources of heat; Thermal resistance; Basic airflow models; Impact on reliability; Altitude Effects.

**Reliability:** Bathtub curves; Highly Accelerated Life Testing (HALT).

**Models and Simulation:** Spice and IBIS-based simulations.


**Advanced Topic Seminars**

This module allows the participation of industry in the teaching of topics of specialist and current interest as they arise from time to time.

This module will address topics of current interest in the VLSI and telecommunications industries as these arise. Suitable topics include:

Advanced architectures for mobile and 3rd generation telecommunications systems.

Advanced topics in networking, such as Voice over IP, Quality of Service provision, bandwidth provisioning and resource reservation.

Radio Frequency VLSI design.

Advances in semiconductor fabrication techniques.

**Master of Engineering Project 1**

To allow the student to gain the experience of undertaking a significant engineering task, which will involve research into a selected topic in the areas of computer, communications or VLSI engineering, along with appropriate advanced design and implementation.

The project is undertaken through the two semesters of the second year of the course. Projects are normally undertaken individually by students (although group project work is also allowed). Each project student (or project group) works under the supervision of an academic staff member who is responsible for the overall direction of the project. The project will be a significant engineering task, involving research, design and implementation related to a selected problem in the areas of computer, communications or VLSI engineering.
Master of Engineering Project 2

To allow the student to gain the experience of undertaking a significant engineering task, which will involve research into a selected topic in the areas of computer, communications or VLSI engineering, along with appropriate advanced design and implementation.

The project is undertaken through the two semesters of the second year of the course. Projects are normally undertaken individually by students (although group project work is also allowed). Each project student (or project group) works under the supervision of an academic staff member who is responsible for the overall direction of the project. The project will be a significant engineering task, involving research, design and implementation related to a selected problem in the areas of computer, communications or VLSI engineering.